



97.469
IC Design Project

5-Bit Pseudo-Random Bit Generator with Clock Generator

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Pat Suwalski
294246

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INTRODUCTION

The goal of the project was to become familiar with the design techniques and tools used to create integrated circuits.

The main design consists of 5 flip-flops with a X-Nor gate feedback combining the output of the first and last flip-flops. Additionally, an on-chip clock generator was added to split the main clock input into two complementary signals. Remaining space is filled in with input protection and output buffers.

The design is entirely NMOS, with a minimum feature size of $5\mu\text{m}$. The total size of the integrated circuit is 230λ by 230λ , which is equivalent to 0.575mm by 0.575mm .

DESIGN OVERVIEW

Block Diagram

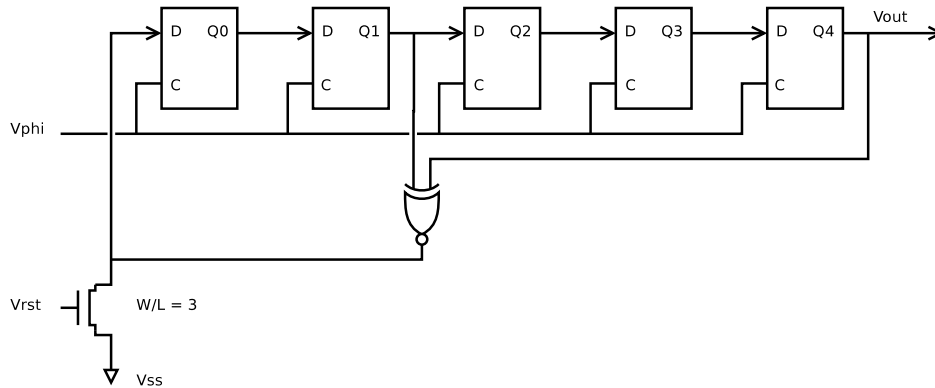


Figure 1 - Block Diagram of IC.

The overall design consists of 5 cascading flip-flops with X-Nor feedback of the output of the first flip-flop with the last one. The flip-flops can be reset through the reset transistor.

Bit Sequence

Q_0	Q_1	Q_2	Q_3	V_{out} Q_4
0	0	0	0	0
1	0	0	0	0
1	1	0	0	0
0	1	1	0	0
0	0	1	1	0
1	0	0	1	1
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0
0	1	1	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0
0	1	1	1	1
1	0	1	1	1
0	1	0	1	1
1	0	1	0	1
0	1	0	1	0
0	0	1	0	1
0	0	0	1	0
1	0	0	0	1
0	1	0	0	0
0	0	1	0	0
1	0	0	1	0
1	1	0	0	1
1	1	1	0	0
0	1	1	1	0
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1

The sequence produced by this project is $2^5 - 1 = 31$ iterations long, after which the pattern repeats. The sequence visible to a probe on V_{out} is the output from Q_4 , the last flip-flop. The Xor expression for Q_0 can be represented as:

$$Q_0 = \overline{Q_1 + Q_2}$$

CIRCUIT SCHEMATICS

Top-Level Schematic

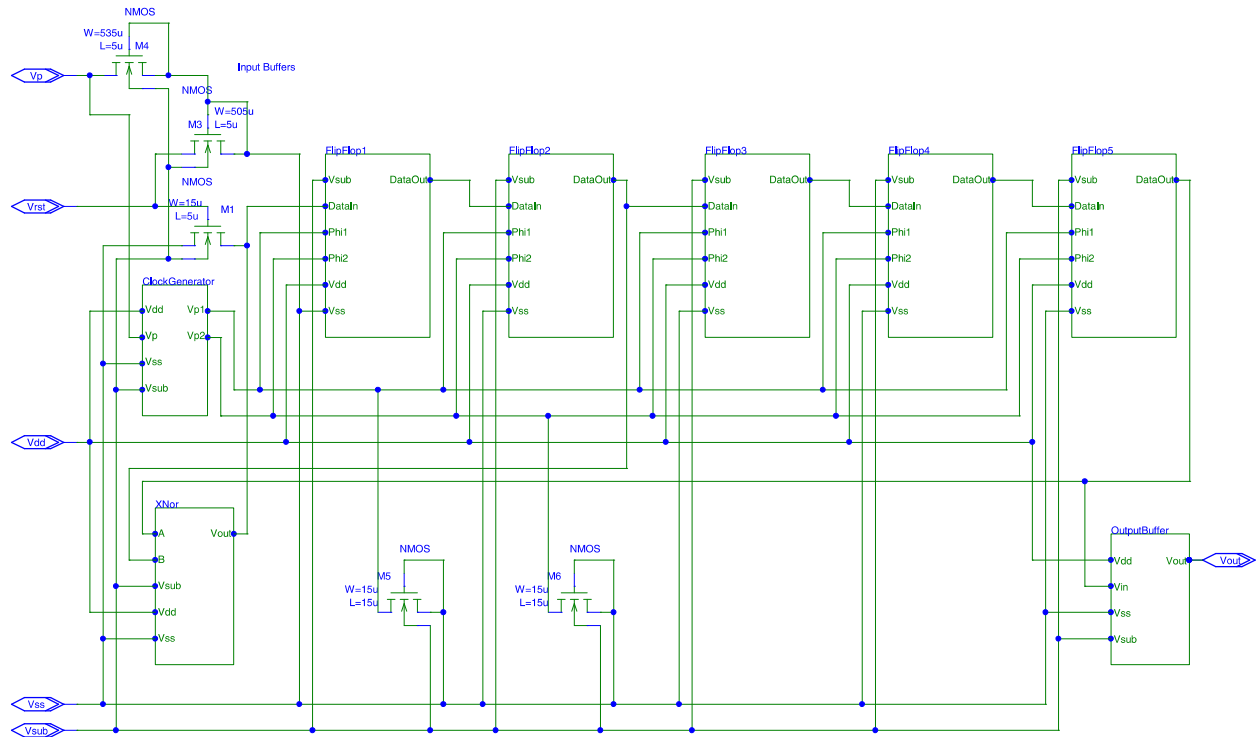


Figure 2 - Schematic of the top-level design.

Flip-Flop

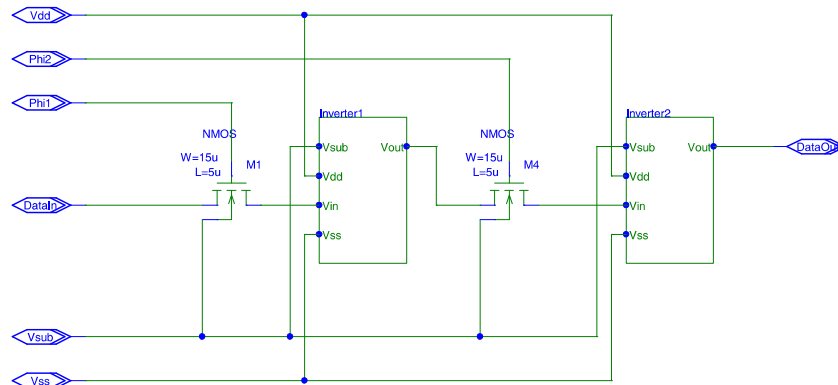


Figure 3 - Schematic of a flip-flop block.

X-Nor

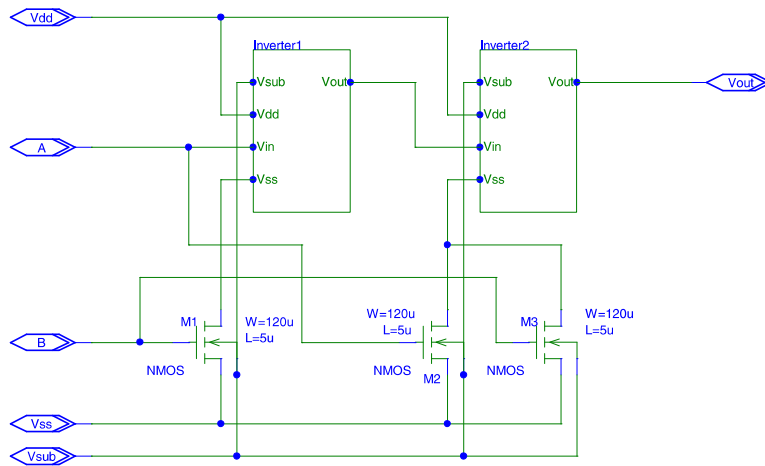


Figure 4 - Schematic of X-Nor block.

Clock Generator

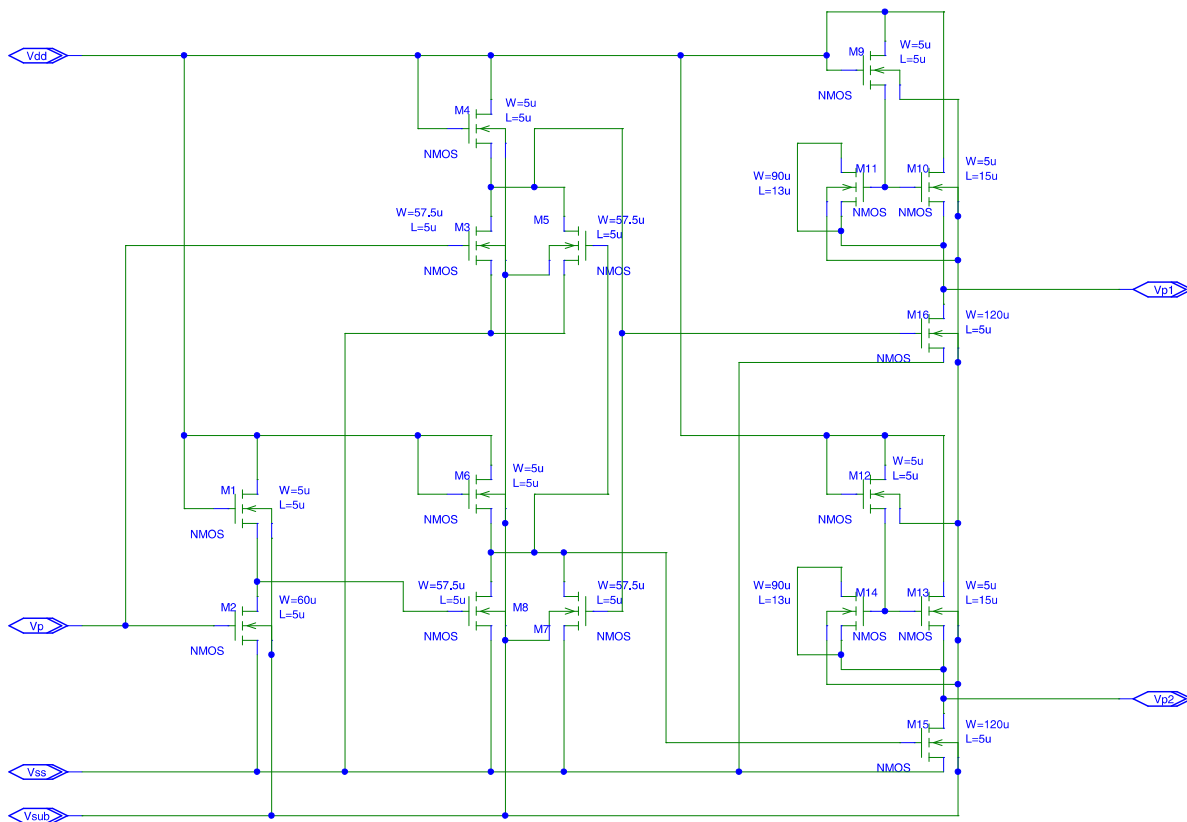


Figure 5 - Schematic of Clock Generator block.

Inverter with 12:1 Pull-down

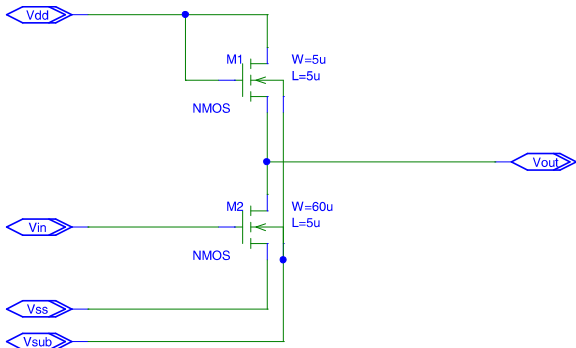


Figure 6 - Schematic of 12:1 Inverter block.

Inverter with 24:1 Pull-down

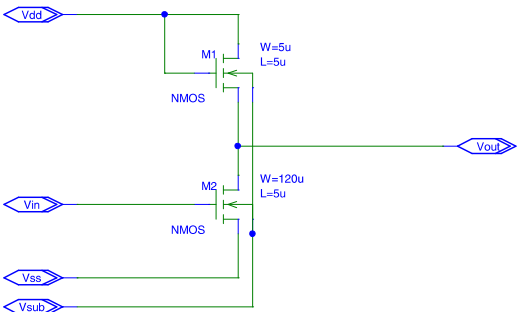


Figure 7 - Schematic of 24:1 Inverter block.

LAYOUT

Overall Layout

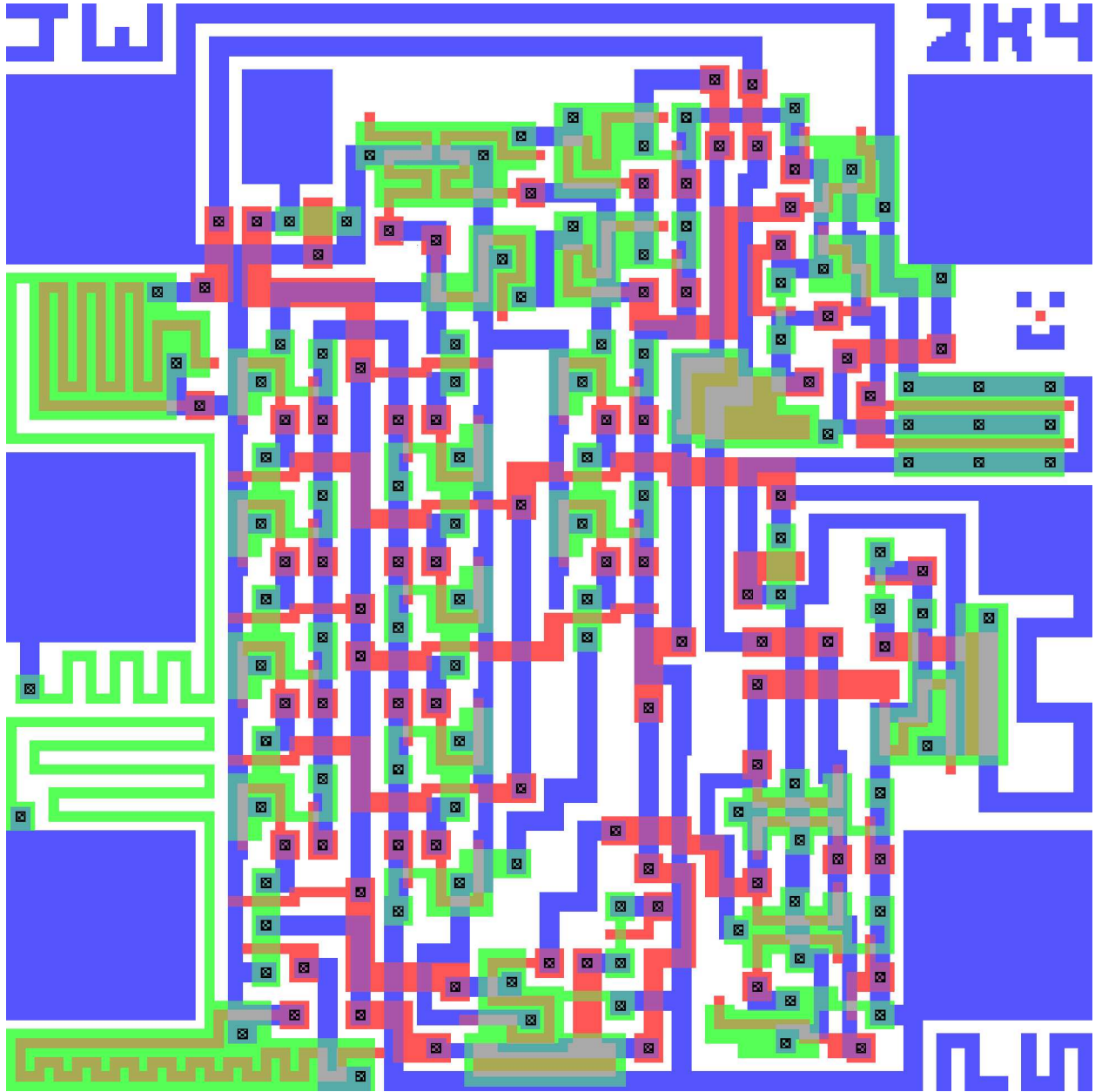


Figure 8 - Complete IC Layout.

Block Design

The layout of the IC is divided into smaller blocks, which allows for easier handling during the layout phase. Additionally, for repeated units, such as the flip-flops and inverters, the blocks save time and guarantee a uniform design, decreasing chances of error due to layout mistakes.

The overall design uses metal wherever possible at the expense of space. To save some space with metal lines, high-density areas, such as the flip-flop blocks, only have one metal line running between them. Much of the interconnection between tightly-placed blocks is achieved using polysilicon. Since this material is more resistive than metal, long poly connections are avoided, and the polysilicon is 6λ wide, or as wide as possible. V_{DD} and V_{SS} never cross through polysilicon. The design is compliant with Mead-Conway design rules.

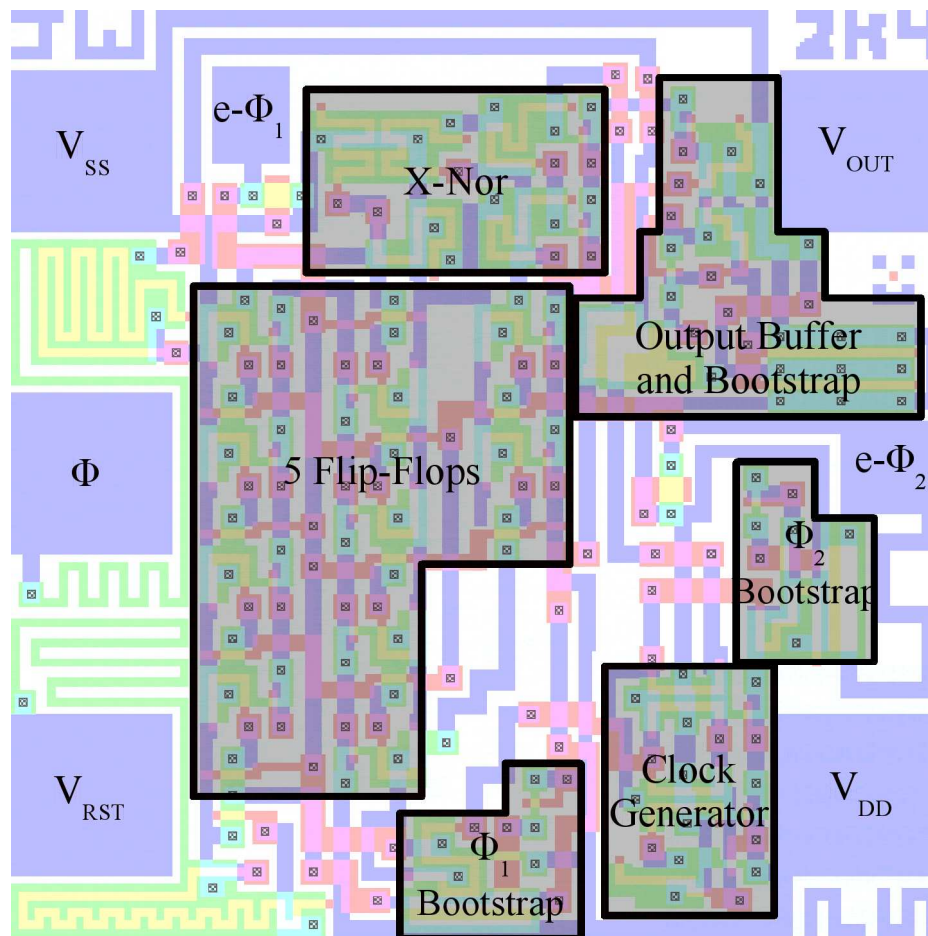


Figure 9 - Annotated Layout

Details regarding space minimization, transistor width-to-length ratio selection, and cell hierarchies of the outlined blocks are described in detail in the following sections.

Flip-Flop Block Layout

The flip-flop (Figure 10) was the first cell created. With a given pull-up transistor width-to-length ratio of 1, the pull-down was designed with a ratio of 12.

The cell contains two cells within it, both 12:1 ratio inverters. The design was initially substantially larger, with pads for the V_{p1} and V_{p2} clock signals, but the design was compressed when it became more practical to join the clocks on adjacent cells directly with polysilicon. This also allowed for more flexibility in placing the pads.

Also removed in the area reduction were the input and output pads on the top-most and bottom-most wells. This allowed for a more compact layout because one flip-flop could feed into the next without the use of metal.

With the reduced layout, the five flip-flops went from occupying approximately one-half of the layout to an estimated third.

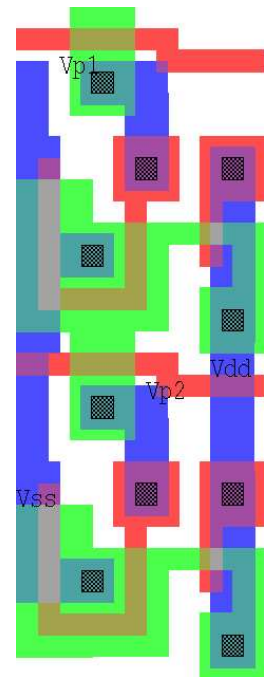


Figure 10 - Flip-Flop Layout

X-Nor Block Layout

The X-Nor design (Figure 11) was provided with minimum geometry pull-up transistors. This design necessitated large pull-down transistors to maintain similar rise and fall times on the output waveforms. The final design has pull-down transistors with a width-to-length ratio of 48. The large size of the pull-down transistors made this unit difficult to lay out and later place. Generally, a smaller design with far fewer transistors would be possible.

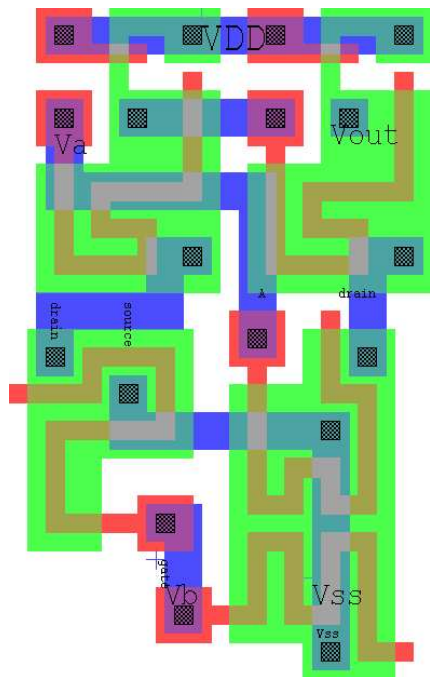


Figure 11 - X-Nor Layout

With this design, the two top cells are the same block. This design could have been more optimized for space by joining the well of the transistor in the bottom-left to the adjacent transistors. Also, the two bottom transistors could have had their polysilicon joined directly, rather than via metal. However, since there is only one instance of the X-Nor block, the space savings would have been minimal. This design was not further reduced because, once placed, the unit fit nicely in the overall layout.

The most cumbersome aspect of the design is the location of the V_{out} pad. Due to the amount of required metal in the design, the output can only exit the block through one side. This proved difficult feed back to the flip-flop cells. This could have been improved by not using identical inverter cells, and instead having the pad labeled V_a attached directly via polysilicon to the bottom-right transistor's gate. V_{out} could then exit the block where there is currently metal.

Clock Generator

The clock generator (Figure 12) is an additional block added to the IC to allow for on-chip clock generation. For the flip-flops to alternate properly, there must be two alternating clocks. As such, the clock generator takes a single clock (V_p) and splits it into V_{p1} and V_{p2} via two cross-coupled Nor gates (Figure 13). Since the clocks are drawn by multiple loads, V_{p1} and V_{p2} are bootstrapped to ensure good signal levels.

The design of this block is as compact as possible, as it was added toward the end of the overall design. The difficulty in the design lies in crossing the outputs of the two Nor blocks. This was accomplished by making the V_{p1} output in polysilicon.

The uniformity of the design is largely due to the three pull-up transistors being of minimum geometry, while all of the other transistors line up because they are all equally sized at a width-to-length ratio of 12-to-1.

In the event that the clock generator did not work, emergency pads were placed the layout where V_{p1} and V_{p2} could be provided for externally. These are labeled $e-\Phi_1$ and $e-\Phi_2$ on Figure 9. Both have minimal input protection, and V_{p2} can be severed via a serpentine metal trace just above the V_{DD} contact pad.

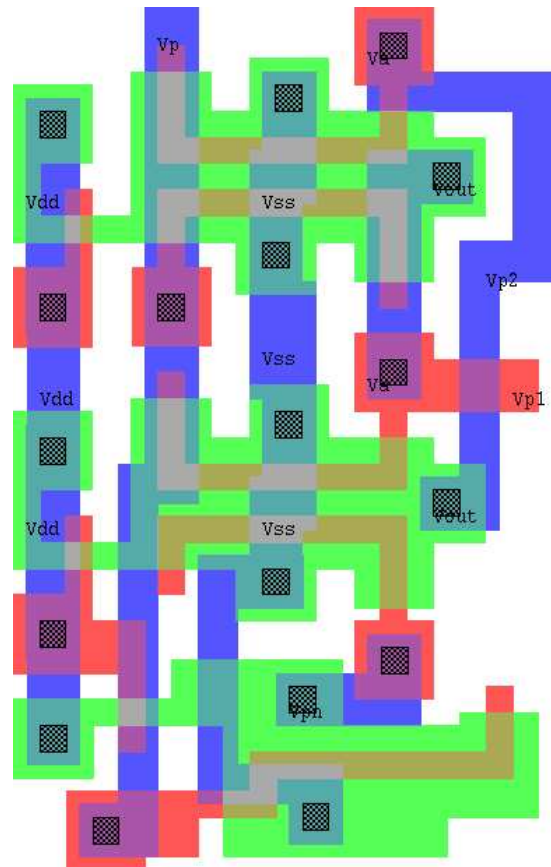


Figure 12 - Clock Generator Layout.

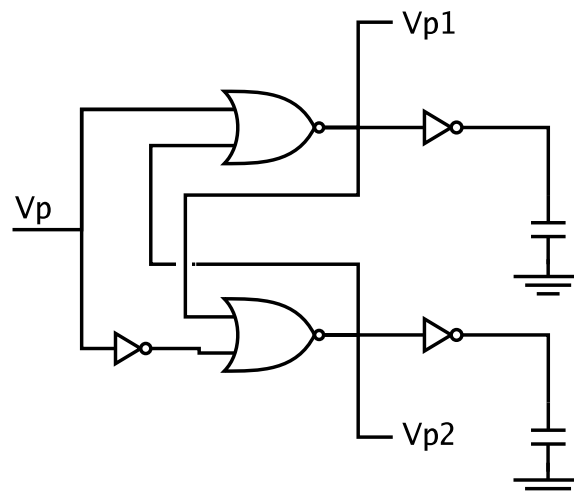


Figure 13 - Clock Generator Schematic.

Input Protection

Input protection to the IC is provided using a long, resistive channel of device well, with a large transistor whose gate and source are grounded at the end. Output is taken at the drain of this transistor. The device well resistor is meant to dissipate a voltage spike, while the large transistor is designed to go into breakdown and ground what remains of the spike. In normal operation, the transistor does not affect the input signal.

The inputs for V_{rst} and V_p use input protection. Not much design work went into these units; any space that could be used was used.

Output Protection

The output protection consists of a two stage output buffer. While a three stage would fit physically, the buffer must consist of an even number of stages, since each stage inverts the signal, and thus an even number is required to produce the correct sequence on V_{out} .

The general rule governing the size of output buffer inverters is to set $f = 3$, and scale according to:

$$\left(\frac{W}{L}\right)_{n, pu} = f^{n-1} \quad \text{and} \quad \left(\frac{W}{L}\right)_{n, pd} = 12 f^{n-1}$$

Using these equations, the first stage of the output buffer (Figure 16) is an inverter with a minimum geometry pull-up, and a 12:1 pull-down transistor. Initially, one of the inverter blocks used elsewhere in the design was used, but due to spatial concerns, it was replaced with a unit that could feed more readily into the next stage.

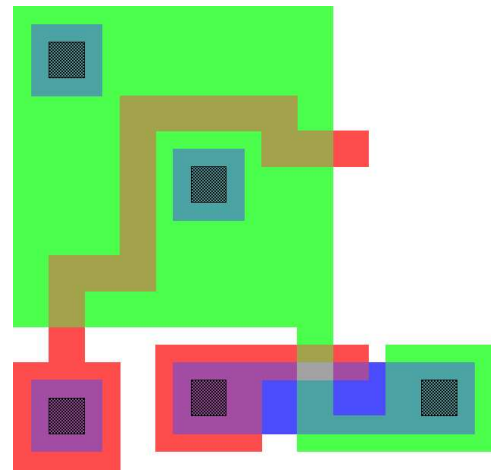


Figure 16 - Output Buffer Stage 1.

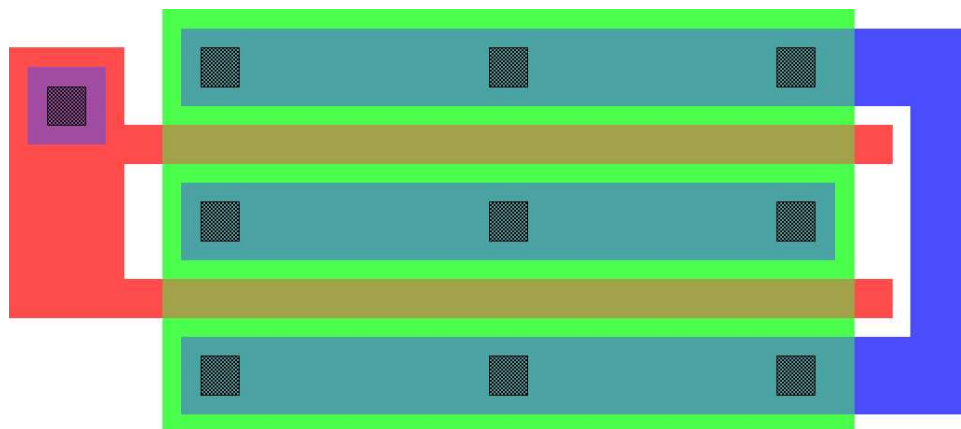


Figure 17 - Output Buffer Stage 2 Pull-down.

The second stage of the output buffer (Figure 17), is designed to have a pull-down transistor with a width-to-length ratio of 36:1. For this design to be practical, a fork layout was used. As this is the final stage, V_{out} is attached to the drain, which is the middle strip of metal.

The pull-up transistor for stage 2 is in a block along with the driver for the bootstrap capacitor (Figure 18). The proper width-to-length ratio for this transistor is 6:1, however, the ratio is actually 9:1. This is because in the initial design, the stage 2 pull-down transistor was 150% the size of the final design. Once that transistor was reduced to the correct size, this one was neglected. Since the pull-up is responsible for the rising edge of the output, this design suffers from a slower signal rise time than fall time. This is discussed further in the testing sections of this report.

The criteria for the bootstrap capacitor is that it be as large as feasibly possible on the layout. Therefore, the bootstrap capacitor was expanded beyond its original rectangular shape into one specifically designed to fit tightly into the overall layout without breaking any design rules. The result is a large capacitor with an odd shape whose area is mostly under a bus of metal traces.

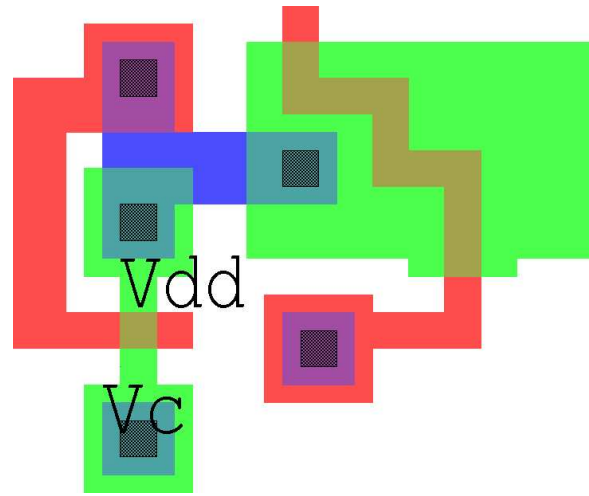


Figure 18 - Output Buffer Stage 2 Pull-up, and Driver for Bootstrap Capacitor.

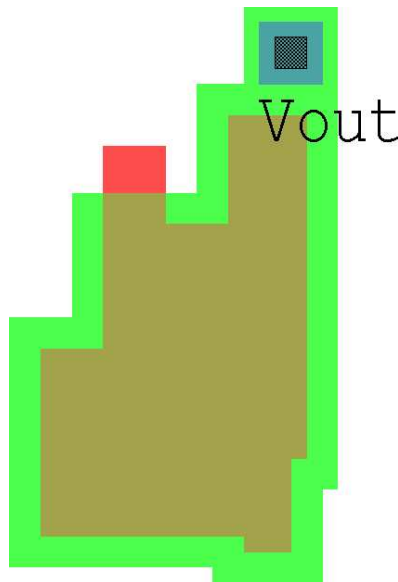


Figure 19 - Bootstrap Capacitor Layout.

CIRCUIT EXTRACTION AND SIMULATION

Throughout the design phase of both the schematic and layout, the output was constantly compared for consistency by running PSPICE simulations. To ensure the consistency of results, and to save time after each netlist extraction, the simulation was sourced out into a separate file that was included in each simulation. This approach also allowed for a number of clock settings that could be easily uncommented as needed.

Simulation File

```
Vsub 999 0 DC -2
Vss Vss 0 DC 0
Vdd Vdd Vss DC 5

* PULSE: LOW HIGH DELAY RISE FALL ONTIME PERIOD

* 10 KHz ---
Vrst Vrst Vss PULSE (0 5 0N 0.1U 0.1U 400U 0N)
Vp Vp Vss PULSE (0 5 0 0.1U 0.1U 50U 100U)
.TRAN 100N 4.5m

* 2 MHz ---
* Vrst Vrst Vss PULSE (0 5 0N 0.1U 0.1U 2000n 0N)
* Vp Vp Vss PULSE (0 5 0 0.1U 0.1U 250n 500n)
* .TRAN 10N 20U

* 4 MHz ---
* Vrst Vrst Vss PULSE (0 5 0N 0.1U 0.1U 1000n 0N)
* Vp Vp Vss PULSE (0 5 0 0.1U 0.1U 125n 250n)
* .TRAN 5N 10U

* 8 MHz ---
* Vrst Vrst Vss PULSE (0 5 0N 0.05U 0.05U 500n 0N)
* Vp Vp Vss PULSE (0 5 0 10n 10n 62.5n 125n)
* .TRAN 2.5N 5U

* 18 MHz ---
* Vrst Vrst Vss PULSE (0 5 0N 0.04U 0.04U 180n 0N)
* Vp Vp Vss PULSE (0 5 0 5n 5n 27.5n 55n)
* .TRAN 1.1N 2.2U

* 20 MHz ---
* Vrst Vrst Vss PULSE (0 5 0N 0.04U 0.04U 200n 0N)
* Vp Vp Vss PULSE (0 5 0 5n 5n 25n 50n)
* .TRAN 1N 2U

.MODEL NMOS NMOS LEVEL=2 NSUB=4E15 TOX=50N
.probe
```

Layout vs. Schematic

To ensure that the layout follows the intended design, a layout vs. schematics (LVS) check was executed. To eliminate most area counting differences, the area comparator was set to a tolerance of 15%. The results are available in Appendix C.

Even with a 15% tolerance, one of the output buffer transistors does not match. This is because it is fairly short and has many corners, which are calculated differently in the layout output, though not by much.

Full-Sequence Output

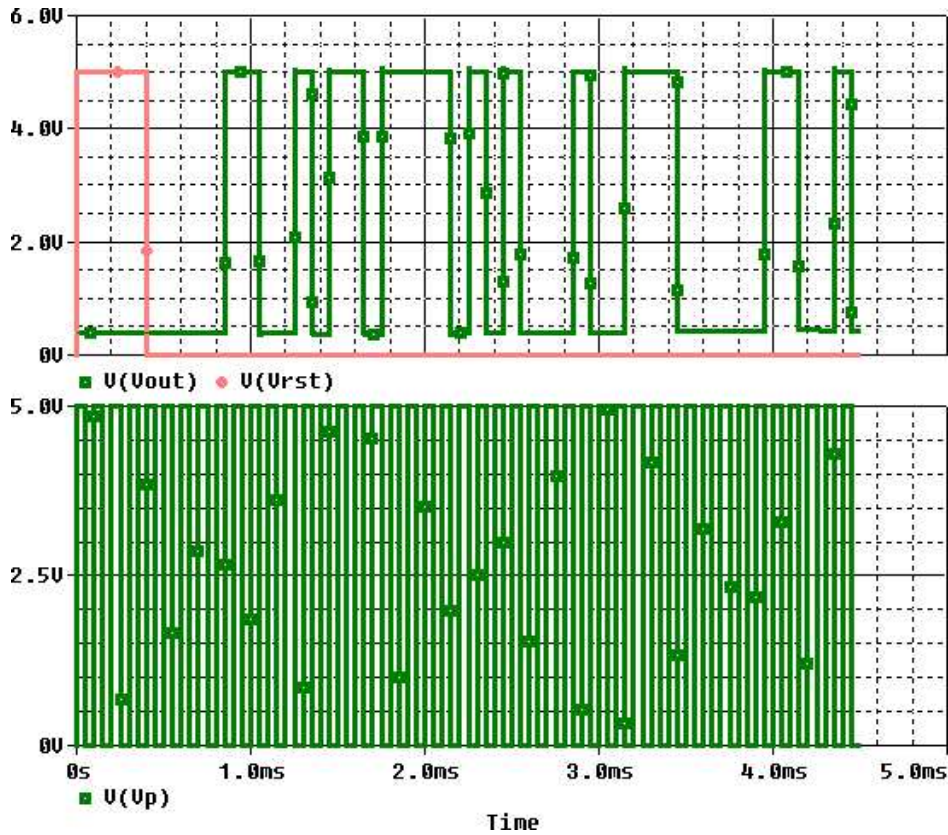


Figure 20 - Full-sequence output ($f=10\text{KHz}$).

The V_{out} signal in Figure 20 shows a full output sequence, as well as several bits of a second sequence. The figure includes the clock signal (V_p) and the reset pulse (V_{rst}). The bit pattern corresponds with the expected output.

During all layout extraction testing, a 10pF load capacitor (C_L) was added to the SPICE source as follows:

```
CLoad Vout Vss 10pF
```

Output High and Low Levels

From the output plot in Figure 20, the V_{out} output high level is exactly 5V, and the low level is 0.38V. While the output low level should be approximately 0.2V, V_{OL} is proportional to the current in the pull-up transistor to the current in the pull-down transistor. Since the pull-up in the output bootstrap is 150% as wide as it should be, the output level is higher as well, though not significantly enough to cause harm. The high voltage, at 5V, is as expected, due to the bootstrapping. Before the output buffer was in place it was 3.8V.

Output Rise and Fall Times

The output rise and fall times were not completely symmetric, most likely due to the imbalance of transistor ratios on the output buffer. This was not initially noticed because during initial testing, without a 10pF load, the rise and fall times were both instantaneous.

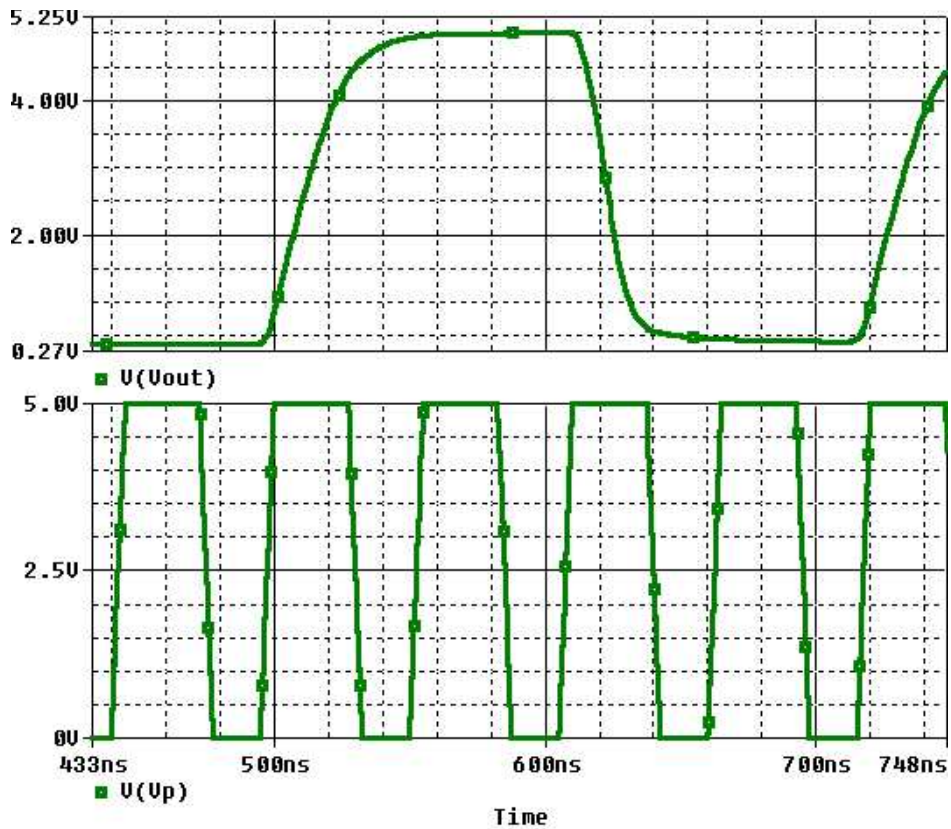
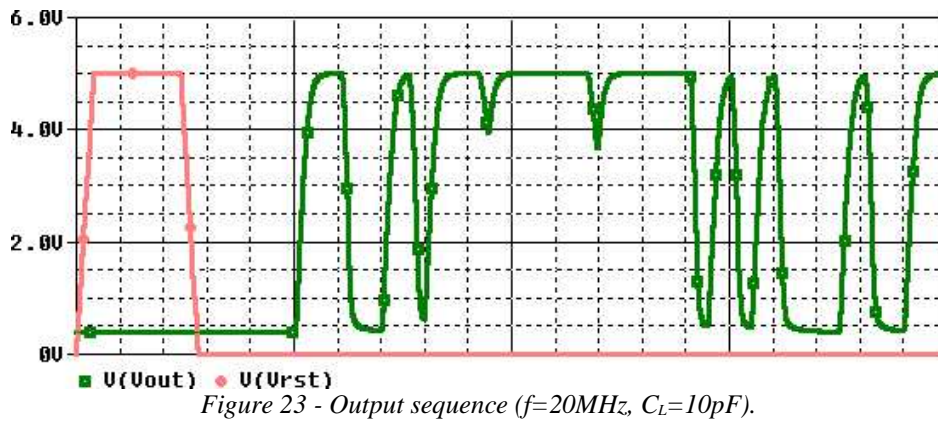
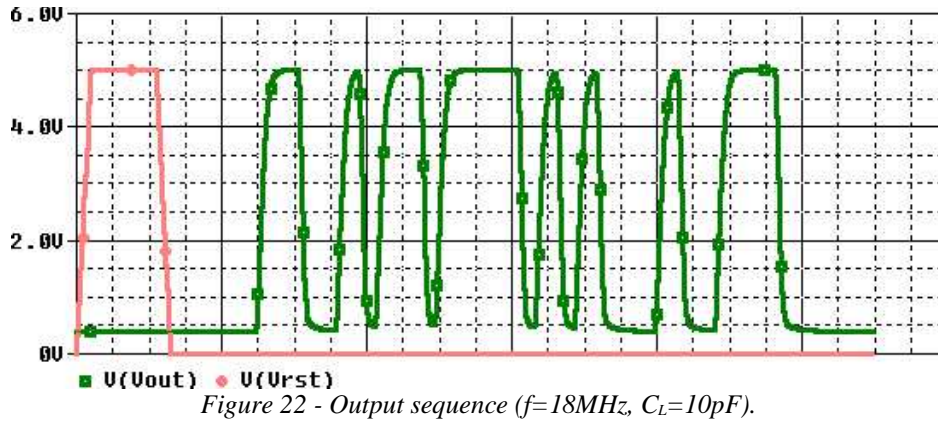


Figure 21 - Enlarged signal transition ($f=18\text{MHz}$, $C_L=10\text{pF}$).

The output rise time (from 10% to 90%) is approximately 30ns, and the fall time with the same parameters is 20ns.

Maximum Useful Clock Frequency

Once the design was finalized the simulation was tested at various frequencies. In theory, with the longest logic change time being 30ns, the IC could clock up to approximately 30MHz. However, signals inside the chip are not as fast as the final output and the unit fails at a lower clock frequency.



While the output waveform is still well-defined at 18MHz, by the time the clock is raised to 20MHz, the low level is not low enough to produce the proper sequence. As a result, several additional states are added in the middle of the output. The IC is no longer reliable.

Glitching in Simulation

The output-buffered simulation did not show signs of glitching. However, before the buffer was in place, there were signs of glitching in excess of 1V. These were on the clock changes and can likely be attributed to the instantaneous indeterminate state while the clocks flip.

Clock Generator Simulation

Before the clock generator was fully integrated into the project, unit testing was performed to see that it worked correctly.

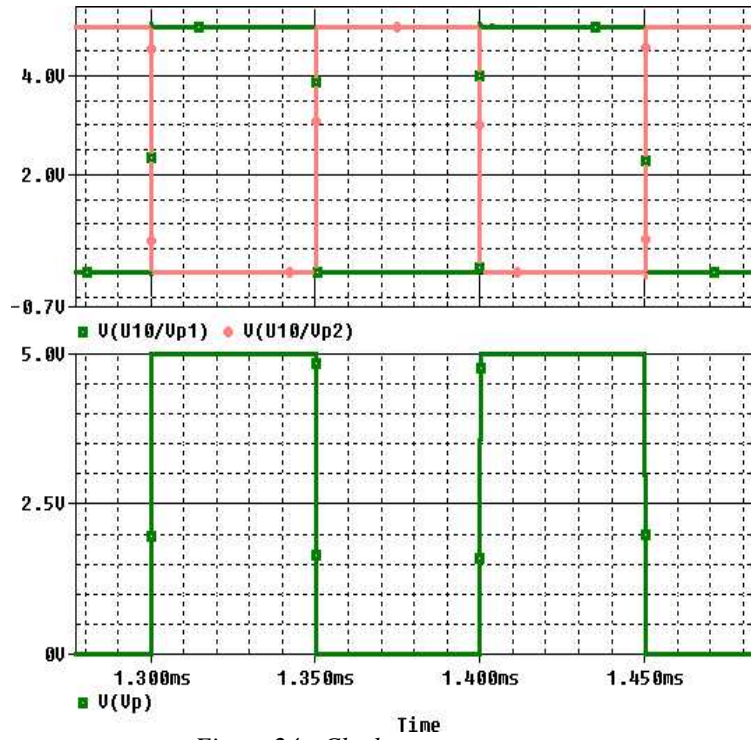


Figure 24 - Clock generator output.

The clock generator works as expected, taking the input clock signal (Figure 24, bottom), and splitting it into two out-of-phase clock signals.

HARDWARE TESTING OF FABRICATED IC

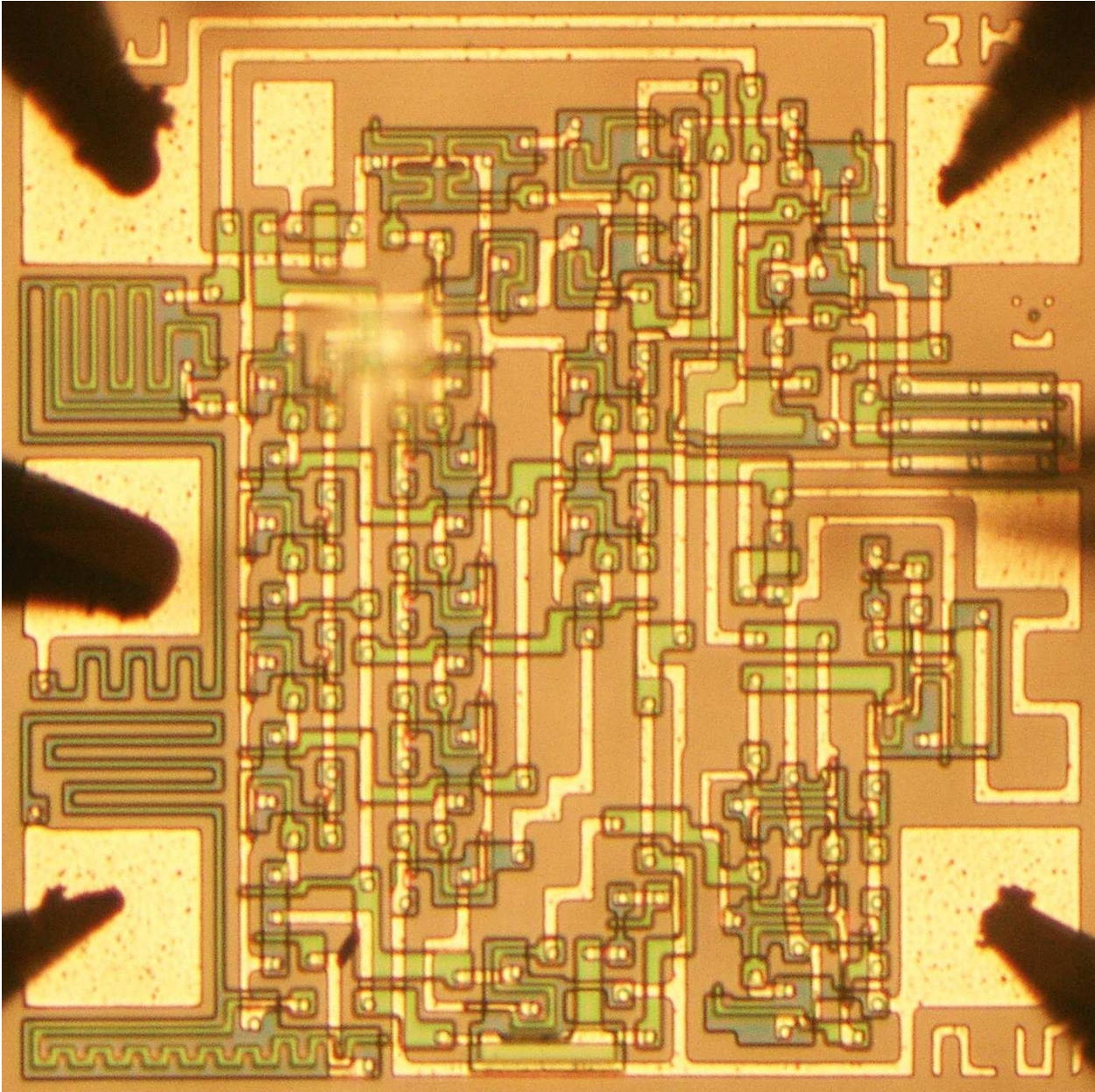


Figure 25 - Photo of IC in testing apparatus (100x magnification).

General Testing Information

Testing of the fabricated IC took place on a testbench designed to probe chips. The chip had its inputs and outputs connected via tungsten needles (Figure 25). Due to the presence of an on-chip clock generator, the middle pin on the right hovers over the wafer and does not make electrical contact with it.

The inputs to the IC were connected to a reliable high-precision voltage source. The clock input was generated by a variable frequency generator set to produce square-shaped pulses with a 50% duty cycle.

The output from the IC was connected to a Tektronix digital oscilloscope, where readings were taken from and waveforms saved.

Output Sequence

The IC was tested by initially setting the clock input to 10KHz and recording the sequence on the oscilloscope.

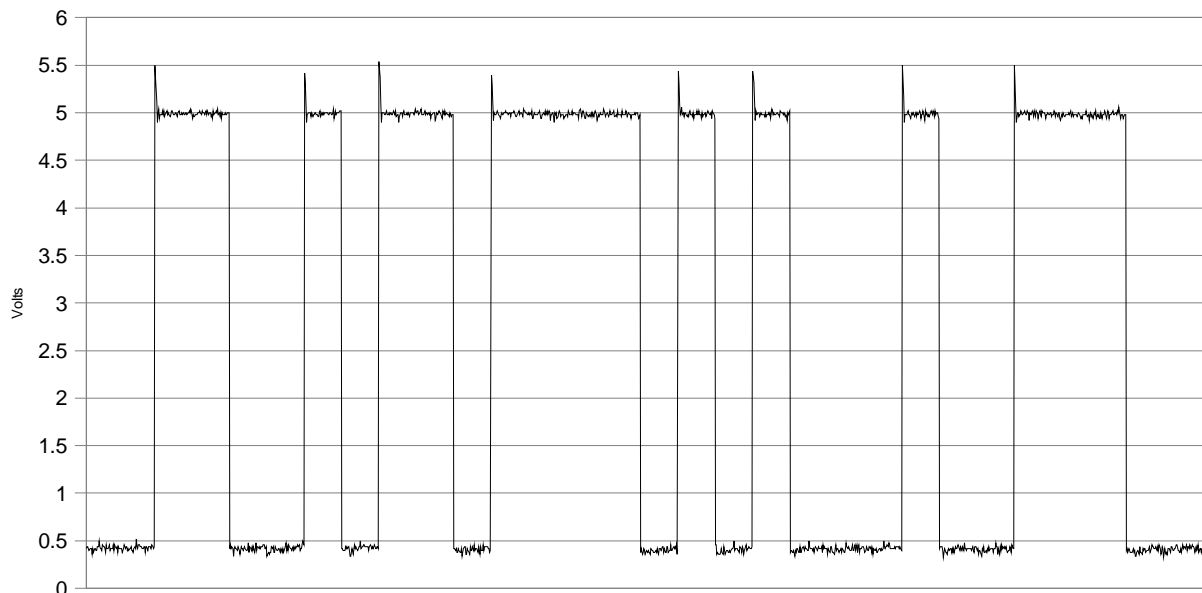


Figure 26 - Full sequence ($f=10\text{KHz}$, $\Delta t=3\text{ms}$).

The output sequence (Figure 26) matches the predicted sequence and the sequence generated by the layout extraction.

Output Levels

An average calculation of over a sequence of low points and high points from the data set collected indicates that output high is at 4.98V and output low is 0.41V. Because the IC is bootstrapped, the value of V_{BB} has no effect on output levels. However, the chip does not work with $V_{BB} = 0V$. This is because this NMOS process relies on substrate voltage biasing.

Rise and Fall Times

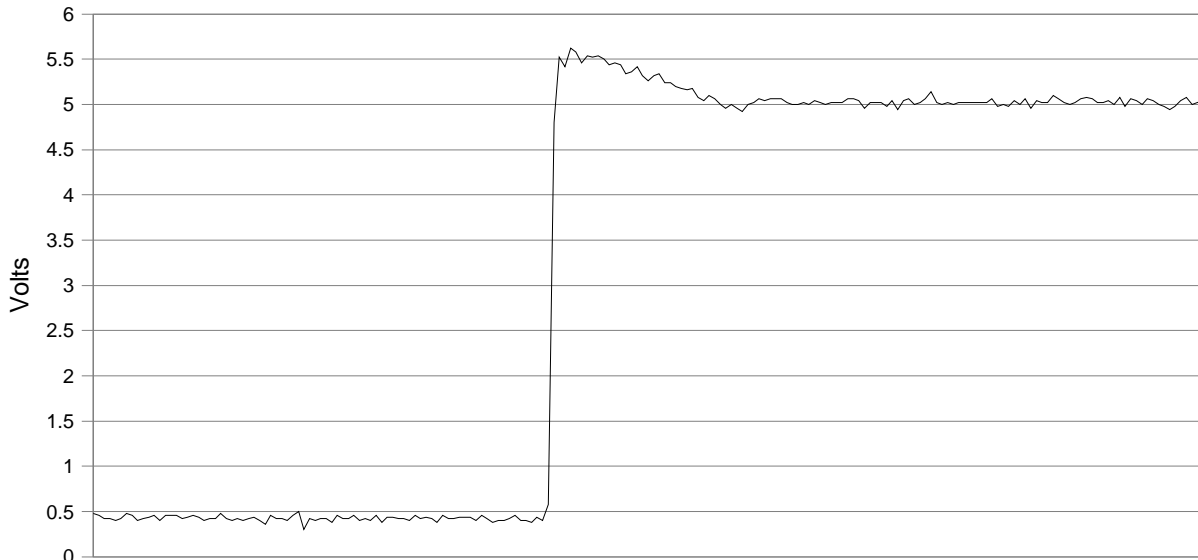


Figure 27 - Typical Rise ($f=10KHz$, $\Delta t=40\mu s$).

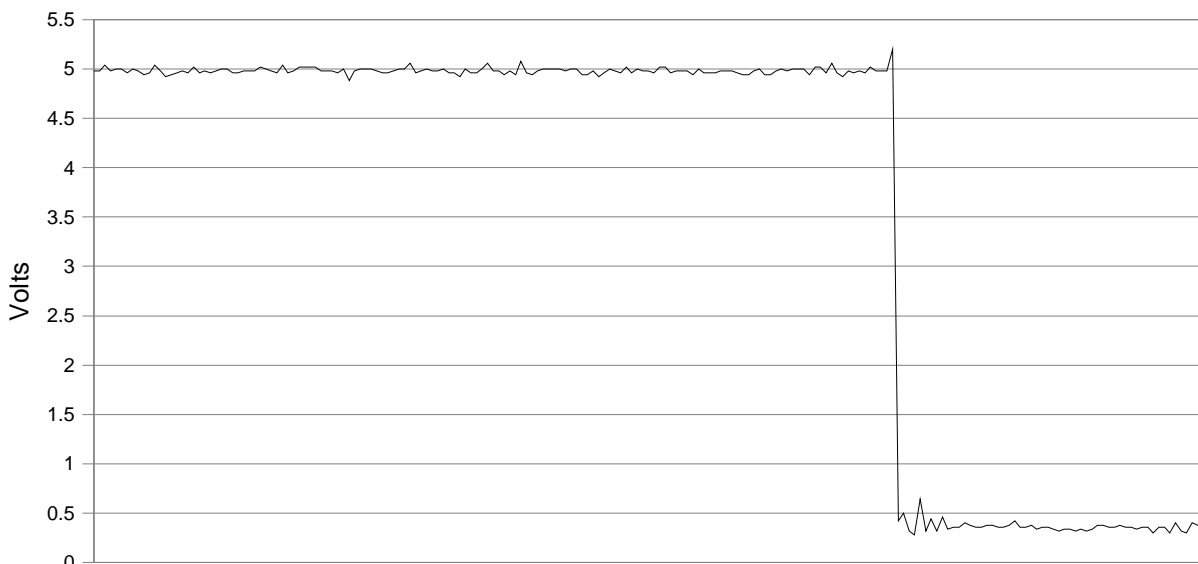


Figure 28 - Typical Fall ($f=10KHz$, $\Delta t=40\mu s$).

Figures 27 and 28 show a typical rise and fall at 10KHz. While these waveforms do not possess the resolution to determine the rise and fall times (resolution is 20 μ s), they do show that it takes 5.8 μ s for the rising pulse to reach a steady state, and it takes 1.6 μ s for the falling pulse to achieve a steady state.

The rise time as claimed by the oscilloscope's internal measurements indicates that the rise time is 99.89ns and the fall time is 400ns. As there is no concrete basis for these results, there is nothing to indicate that these numbers are correct.

The best rise and fall time reading can be made from the data set pertaining to Figure 29 (below). From this high-frequency, high-resolution plot, the rise time is 65.6ns and the fall time is 127.6ns.

Maximum Clock Frequency

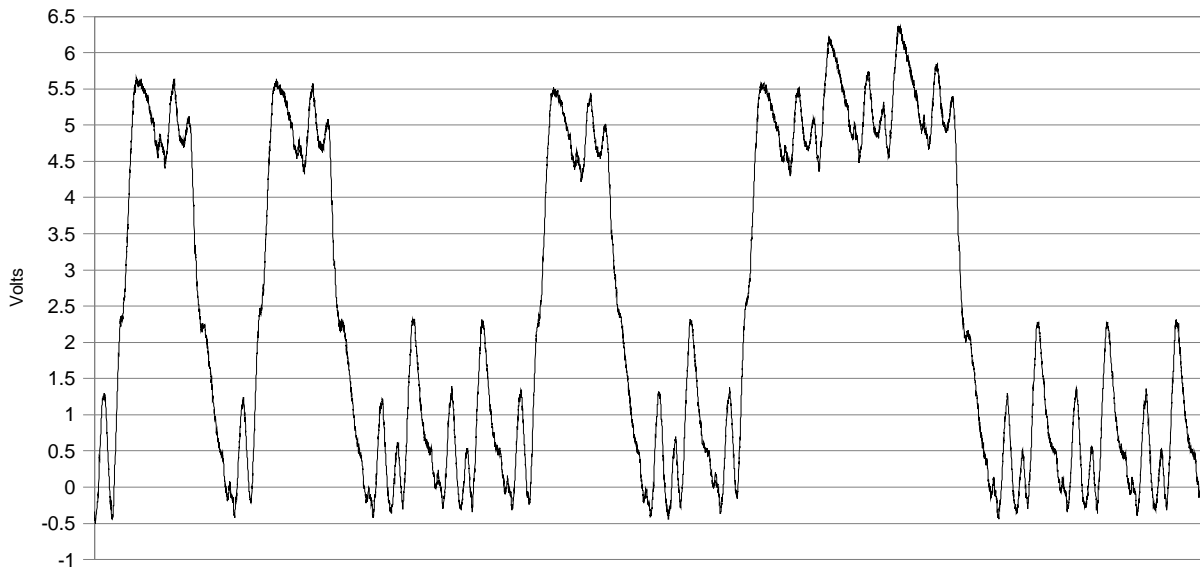


Figure 29 - V_{out} at 4MHz ($\Delta t=4\mu$ s).

The highest clock frequency the IC can sustain is 4MHz. Interestingly, the chip did not work at a clock frequency of 2MHz, though it worked at frequencies both higher and lower.

Hardware vs. Simulation

The overall function of the design worked the same way in simulation and hardware. This indicates that the simulation portrayed the circuit fairly accurately.

There are, however, some discrepancies. Most notably, the maximum clock rate is over four times slower in hardware than in simulation. This is likely linked to the rise and fall times. In simulation, the rise time was 30ns, and in reality it was anywhere between 60ns to 100ns. The fall times were even less accurately predicted, with the simulation indicating 20ns, while the oscilloscope showed 120ns to 400ns. The slower operation of the circuit can possibly be attributed to field effects not accounted for by the simulation.

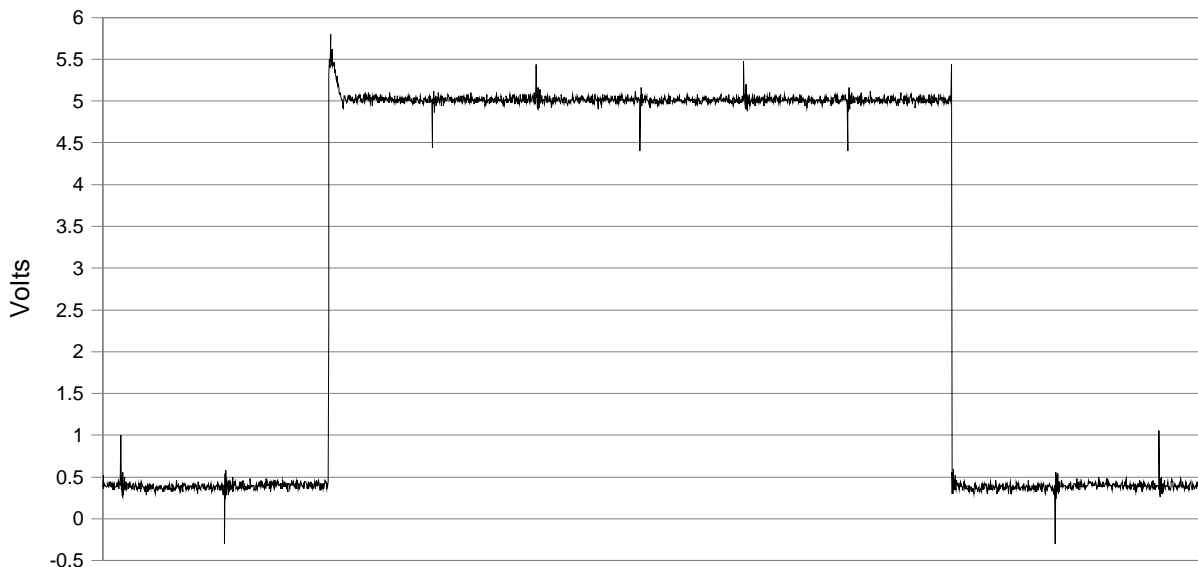


Figure 30 - Typical Output, 3 Clock Cycles High ($f=10\text{KHz}$, $\Delta t=500\mu\text{s}$).

Before the bootstrapping was added, the SPICE simulation would have very large glitching effects, including large overshoots and undershoots on logic level change. While the buffer suppressed this behaviour in simulation, the fabricated IC showed signs of glitching, with spikes up to 0.6V. Since glitches occur on every clock edge, they must be caused by the indeterminate state of the system in between the clocks.

It is interesting that the chip performs very well while switching to logic low level, with no undershoot. On the other hand, the leading edge of the output signal overshoots by 0.6V. This can likely be attributed to the imbalance between the pull-up and pull-down transistor ratios on the final output stage, and their interaction with the bootstrap capacitor. Since the pull-up transistor is very small compared to the capacitor, it cannot quickly suppress the capacitor's surge of current. When the capacitor discharges, the voltage level drops to the expected 5V.

Finally, the simulation correctly predicted logic voltages. While low, both simulated and real logic-0 is $\sim 0.4\text{V}$, rather than the desired 0.2V. This can be a result of the 9:1 ratio of pull-up to pull-down on the final output stage, rather than the desired 12:1.

CONCLUSION

The design and fabrication process of the integrated circuit proceeded quickly and smoothly. The final fabricated chip worked as expected, with all parameters except maximum clock frequency accurate to the simulation.

While not a particularly complex (or useful) integrated circuit, this design project highlighted the procedure and methods that are required to design, test, and produce NMOS chips.

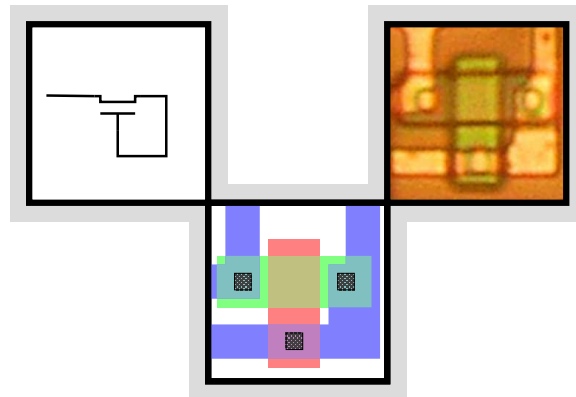


Figure 31 - Process: Schematic, Layout, Fabrication.

APPENDIX A – SCHEMATIC NETLIST

* Schematics Netlist *

.EXTERNAL OUTPUT Vout
.EXTERNAL INPUT Vdd
.EXTERNAL INPUT Vsub
.EXTERNAL INPUT Vrst
.EXTERNAL INPUT Vp
.EXTERNAL INPUT Vss

```
M_FlipFlop2_Inverter1_M1      Vdd Vdd $N_0001 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop2_Inverter1_M2      $N_0001 $N_0002 Vss Vsub NMOS
+ L=5u
+ W=60u
M_FlipFlop2_Inverter2_M1      Vdd Vdd $N_0028 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop2_Inverter2_M2      $N_0028 $N_0003 Vss Vsub NMOS
+ L=5u
+ W=60u
M_FlipFlop2_M1                 $N_0002 $N_0025 $N_0006 Vsub NMOS
+ L=5u
+ W=15u
M_FlipFlop2_M4                 $N_0003 $N_0027 $N_0001 Vsub NMOS
+ L=5u
+ W=15u
M_FlipFlop1_Inverter1_M1      Vdd Vdd $N_0004 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop1_Inverter1_M2      $N_0004 $N_0005 Vss Vsub NMOS
+ L=5u
+ W=60u
M_FlipFlop1_Inverter2_M1      Vdd Vdd $N_0006 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop1_Inverter2_M2      $N_0006 $N_0007 Vss Vsub NMOS
+ L=5u
+ W=60u
M_FlipFlop1_M1                 $N_0005 $N_0025 $N_0033 Vsub NMOS
+ L=5u
+ W=15u
M_FlipFlop1_M4                 $N_0007 $N_0027 $N_0004 Vsub NMOS
+ L=5u
+ W=15u
M_FlipFlop3_Inverter1_M1      Vdd Vdd $N_0008 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop3_Inverter1_M2      $N_0008 $N_0009 Vss Vsub NMOS
+ L=5u
+ W=60u
M_FlipFlop3_Inverter2_M1      Vdd Vdd $N_0011 Vsub NMOS
+ L=5u
+ W=5u
M_FlipFlop3_Inverter2_M2      $N_0011 $N_0010 Vss Vsub NMOS
+ L=5u
+ W=60u
```

M_FlipFlop3_M1	\$N_0009 \$N_0025 \$N_0028 Vsub NMOS
+ L=5u	
+ W=15u	
M_FlipFlop3_M4	\$N_0010 \$N_0027 \$N_0008 Vsub NMOS
+ L=5u	
+ W=15u	
M_FlipFlop4_Inverter1_M1	Vdd Vdd \$N_0012 Vsub NMOS
+ L=5u	
+ W=5u	
M_FlipFlop4_Inverter1_M2	\$N_0012 \$N_0013 Vss Vsub NMOS
+ L=5u	
+ W=60u	
M_FlipFlop4_Inverter2_M1	Vdd Vdd \$N_0015 Vsub NMOS
+ L=5u	
+ W=5u	
M_FlipFlop4_Inverter2_M2	\$N_0015 \$N_0014 Vss Vsub NMOS
+ L=5u	
+ W=60u	
M_FlipFlop4_M1	\$N_0013 \$N_0025 \$N_0011 Vsub NMOS
+ L=5u	
+ W=15u	
M_FlipFlop4_M4	\$N_0014 \$N_0027 \$N_0012 Vsub NMOS
+ L=5u	
+ W=15u	
M_FlipFlop5_Inverter1_M1	Vdd Vdd \$N_0016 Vsub NMOS
+ L=5u	
+ W=5u	
M_FlipFlop5_Inverter1_M2	\$N_0016 \$N_0017 Vss Vsub NMOS
+ L=5u	
+ W=60u	
M_FlipFlop5_Inverter2_M1	Vdd Vdd \$N_0030 Vsub NMOS
+ L=5u	
+ W=5u	
M_FlipFlop5_Inverter2_M2	\$N_0030 \$N_0018 Vss Vsub NMOS
+ L=5u	
+ W=60u	
M_FlipFlop5_M1	\$N_0017 \$N_0025 \$N_0015 Vsub NMOS
+ L=5u	
+ W=15u	
M_FlipFlop5_M4	\$N_0018 \$N_0027 \$N_0016 Vsub NMOS
+ L=5u	
+ W=15u	
M_OutputBuffer_M2	\$N_0019 \$N_0030 Vss Vsub NMOS
+ L=5u	
+ W=60u	
M_OutputBuffer_M1	Vdd Vdd \$N_0019 Vsub NMOS
+ L=5u	
+ W=5u	
M_OutputBuffer_M5	Vout \$N_0020 Vout Vsub NMOS
+ L=20u	
+ W=112.5u	
M_OutputBuffer_M4	Vdd \$N_0020 Vout Vsub NMOS
+ L=5u	
+ W=45u	
M_OutputBuffer_M6	Vdd Vdd \$N_0020 Vsub NMOS
+ L=5u	
+ W=5u	
M_OutputBuffer_M3	Vss \$N_0019 Vout Vsub NMOS
+ L=5u	
+ W=90u	

M_OutputBuffer_M8 + L=5u + W=90u	Vout \$N_0019 Vss Vsub NMOS
M_ClockGenerator_M4 + L=5u + W=5u	Vdd Vdd \$N_0021 Vsub NMOS
M_ClockGenerator_M3 + L=5u + W=57.5u	\$N_0021 Vp Vss Vsub NMOS
M_ClockGenerator_M5 + L=5u + W=57.5u	\$N_0021 \$N_0022 Vss Vsub NMOS
M_ClockGenerator_M1 + L=5u + W=5u	Vdd Vdd \$N_0023 Vsub NMOS
M_ClockGenerator_M2 + L=5u + W=60u	\$N_0023 Vp Vss Vsub NMOS
M_ClockGenerator_M8 + L=5u + W=57.5u	\$N_0022 \$N_0023 Vss Vsub NMOS
M_ClockGenerator_M7 + L=5u + W=57.5u	\$N_0022 \$N_0021 Vss Vsub NMOS
M_ClockGenerator_M9 + L=5u + W=5u	Vdd Vdd \$N_0024 Vsub NMOS
M_ClockGenerator_M11 + L=13u + W=90u	\$N_0025 \$N_0024 \$N_0025 Vsub NMOS
M_ClockGenerator_M10 + L=15u + W=5u	Vdd \$N_0024 \$N_0025 Vsub NMOS
M_ClockGenerator_M16 + L=5u + W=120u	\$N_0025 \$N_0021 Vss Vsub NMOS
M_ClockGenerator_M12 + L=5u + W=5u	Vdd Vdd \$N_0026 Vsub NMOS
M_ClockGenerator_M14 + L=13u + W=90u	\$N_0027 \$N_0026 \$N_0027 Vsub NMOS
M_ClockGenerator_M13 + L=15u + W=5u	Vdd \$N_0026 \$N_0027 Vsub NMOS
M_ClockGenerator_M15 + L=5u + W=120u	\$N_0027 \$N_0022 Vss Vsub NMOS
M_ClockGenerator_M6 + L=5u + W=5u	Vdd Vdd \$N_0022 Vsub NMOS
M_XNor_Inverter1_M2 + L=5u + W=120u	\$N_0032 \$N_0030 \$N_0029 Vsub NMOS
M_XNor_Inverter1_M1 + L=5u + W=5u	Vdd Vdd \$N_0032 Vsub NMOS
M_XNor_Inverter2_M2 + L=5u + W=120u	\$N_0033 \$N_0032 \$N_0031 Vsub NMOS

M_XNor_Inverter2_M1	Vdd Vdd \$N_0033 Vsub NMOS
+ L=5u	
+ W=5u	
M_XNor_M1	\$N_0029 \$N_0028 Vss Vsub NMOS
+ L=5u	
+ W=120u	
M_XNor_M2	\$N_0031 \$N_0030 Vss Vsub NMOS
+ L=5u	
+ W=120u	
M_XNor_M3	\$N_0031 \$N_0028 Vss Vsub NMOS
+ L=5u	
+ W=120u	
M_M4	Vp Vss Vss Vsub NMOS
+ L=5u	
+ W=535u	
M_M3	Vss Vss Vrst Vsub NMOS
+ L=5u	
+ W=505u	
M_M6	\$N_0027 Vss Vss Vsub NMOS
+ L=15u	
+ W=15u	
M_M5	\$N_0025 Vss Vss Vsub NMOS
+ L=15u	
+ W=15u	
M_M1	\$N_0033 Vrst Vss Vsub NMOS
+ L=5u	
+ W=15u	

APPENDIX B – LAYOUT NETLIST

* Circuit Extracted by Tanner Research's L-Edit V7.12 / Extract V4.00 ;
* TDB File: W:\Project\Project, Cell: JW_PS
* Extract Definition File: W:\nmos2002.ext
* Extract Date and Time: 10/18/2004 - 19:31

.INCLUDE("../Simulation.txt")

* NODE NAME ALIASES

* 1 = Vout (200,201)
* 1 = U23/Vout (172,141)
* 2 = Vp (6,121)
* 2 = U21/Vp (175,71)
* 3 = U7/Vout (135,201)
* 4 = Vdd (198,38)
* 4 = U10/Vdd (82,127)
* 4 = U11/Vdd (65,69)
* 4 = U12/Vdd (65,129)
* 4 = U13/Vdd (133,129)
* 4 = U21/Vdd (184,45)
* 4 = U26/Vdd (163,172)
* 4 = U7/VDD (145,184)
* 4 = U9/Vdd (82,67)
* 4 = U21/U0/Vdd (183,35)
* 4 = U21/U1/Vdd (183,60)
* 5 = U26/Vc (161,163)
* 7 = U7/Va (134,170)
* 7 = U7/U3/A (116,191)
* 8 = Vss (5,202)
* 8 = U10/Vss (99,115)
* 8 = U11/Vss (47,81)
* 8 = U12/Vss (47,141)
* 8 = U13/Vss (115,141)
* 8 = U21/Vss (167,48)
* 8 = U7/Vss (84,196)
* 8 = U9/Vss (99,55)
* 8 = U21/U0/Vss (166,35)
* 8 = U21/U1/Vss (166,60)
* 8 = U7/U3/Vss (79,199)
* 9 = U21/Vp1 (148,44)
* 9 = U21/U0/Va (157,45)
* 9 = U21/U1/Vout (154,60)
* 11 = U10/Vp2 (88,125)
* 11 = U11/Vp2 (59,71)
* 11 = U12/Vp2 (59,131)
* 11 = U13/Vp2 (127,131)
* 11 = U9/Vp2 (88,65)
* 13 = U21/Vp2 (150,53)
* 13 = U21/U0/Vout (154,35)
* 13 = U21/U1/Va (157,70)
* 14 = U21/Vpn (165,20)
* 25 = U7/Vb (85,184)
* 26 = U7/U3/drain (116,203)
* 27 = U7/U0/drain (114,167)
* 27 = U7/U0/source (114,175)
* 30 = U10/Vp1 (96,155)
* 30 = U11/Vp1 (51,41)
* 30 = U12/Vp1 (51,101)

```

*      30 = U13/Vp1 (119,101)
*      30 = U9/Vp1 (96,95)
*      31 = Vrst (5,41)

M1 U26/Vc Vdd Vdd 999 NMOS L=5u W=5u
* M1 DRAIN GATE SOURCE BULK (163 164 165 166)
M2 Vout U26/Vc Vdd 999 NMOS L=5u W=55u
* M2 DRAIN GATE SOURCE BULK (172 168 183 181)
M3 Vout U26/Vc Vout 999 NMOS L=19.3889u W=112.5u
* M3 DRAIN GATE SOURCE BULK (142 138 170 155)
M4 Vss U7/Va 6 999 NMOS L=5u W=72.5u
* M4 DRAIN GATE SOURCE BULK (171 186 184 202)
M5 28 U7/Va U7/U0/drain 999 NMOS L=5u W=135u
* M5 DRAIN GATE SOURCE BULK (118 168 138 184)
M6 6 Vdd Vdd 999 NMOS L=5u W=5u
* M6 DRAIN GATE SOURCE BULK (168 200 170 202)
M7 Vss 6 Vout 999 NMOS L=5u W=90u
* M7 DRAIN GATE SOURCE BULK (188 136 224 138)
M8 Vout 6 Vss 999 NMOS L=5u W=90u
* M8 DRAIN GATE SOURCE BULK (188 144 224 146)
M9 Vss Vss U10/Vp2 999 NMOS L=15u W=15u
* M9 DRAIN GATE SOURCE BULK (161 108 167 114)
M10 10 Vdd Vdd 999 NMOS L=5u W=5u
* M10 DRAIN GATE SOURCE BULK (129 32 131 34)
M11 Vdd 10 U10/Vp1 999 NMOS L=15u W=5u
* M11 DRAIN GATE SOURCE BULK (120 19 126 21)
M12 U10/Vp1 10 U10/Vp1 999 NMOS L=12.6316u W=95u
* M12 DRAIN GATE SOURCE BULK (99 3 129 12)
M13 Vss U21/Vp1 U10/Vp1 999 NMOS L=5u W=135u
* M13 DRAIN GATE SOURCE BULK (100 10 116 28)
M14 12 Vdd Vdd 999 NMOS L=5u W=5u
* M14 DRAIN GATE SOURCE BULK (184 107 186 109)
M15 U10/Vp2 12 U10/Vp2 999 NMOS L=15u W=80u
* M15 DRAIN GATE SOURCE BULK (201 71 210 97)
M16 Vdd 12 U10/Vp2 999 NMOS L=15u W=5u
* M16 DRAIN GATE SOURCE BULK (191 91 193 97)
M17 U10/Vp2 U21/Vp2 Vss 999 NMOS L=5u W=135u
* M17 DRAIN GATE SOURCE BULK (185 69 201 87)
M18 Vss Vss U10/Vp1 999 NMOS L=15u W=15u
* M18 DRAIN GATE SOURCE BULK (63 181 69 187)
M19 Vss Vss Vp 999 NMOS L=5u W=535u
* M19 DRAIN GATE SOURCE BULK (7 144 43 171)
M20 Vss Vp U21/Vp1 999 NMOS L=5u W=65u
* M20 DRAIN GATE SOURCE BULK (158 51 177 58)
M21 Vss U21/Vp2 U21/Vp1 999 NMOS L=5u W=65u
* M21 DRAIN GATE SOURCE BULK (158 60 177 67)
M22 Vdd Vdd U21/Vp1 999 NMOS L=5u W=5u
* M22 DRAIN GATE SOURCE BULK (182 54 184 56)
M23 Vss U21/Vpn U21/Vp2 999 NMOS L=5u W=65u
* M23 DRAIN GATE SOURCE BULK (158 26 177 33)
M24 Vss U21/Vp1 U21/Vp2 999 NMOS L=5u W=65u
* M24 DRAIN GATE SOURCE BULK (158 35 177 42)
M25 Vdd Vdd U21/Vp2 999 NMOS L=5u W=5u
* M25 DRAIN GATE SOURCE BULK (182 29 184 31)
M26 Vdd Vdd U21/Vpn 999 NMOS L=5u W=5u
* M26 DRAIN GATE SOURCE BULK (178 17 180 19)
M27 U21/Vpn Vp Vss 999 NMOS L=5u W=70u
* M27 DRAIN GATE SOURCE BULK (150 10 172 18)
M28 Vss 15 U7/Va 999 NMOS L=5u W=65u
* M28 DRAIN GATE SOURCE BULK (117 143 127 155)

```

M29 Vdd Vdd U7/Va 999 NMOS L=5u W=5u
* M29 DRAIN GATE SOURCE BULK (132 147 134 149)
M30 Vss 16 38 999 NMOS L=5u W=65u
* M30 DRAIN GATE SOURCE BULK (117 113 127 125)
M31 Vdd Vdd 38 999 NMOS L=5u W=5u
* M31 DRAIN GATE SOURCE BULK (132 117 134 119)
M32 29 U10/Vp1 16 999 NMOS L=5u W=15u
* M32 DRAIN GATE SOURCE BULK (120 99 126 101)
M33 18 U10/Vp1 37 999 NMOS L=5u W=15u
* M33 DRAIN GATE SOURCE BULK (92 93 98 95)
M34 15 U10/Vp2 38 999 NMOS L=5u W=15u
* M34 DRAIN GATE SOURCE BULK (120 129 126 131)
M35 19 U10/Vp2 36 999 NMOS L=5u W=15u
* M35 DRAIN GATE SOURCE BULK (92 123 98 125)
M36 23 U10/Vp2 35 999 NMOS L=5u W=15u
* M36 DRAIN GATE SOURCE BULK (52 129 58 131)
M37 Vss 17 29 999 NMOS L=5u W=65u
* M37 DRAIN GATE SOURCE BULK (91 39 101 51)
M38 29 Vdd Vdd 999 NMOS L=5u W=5u
* M38 DRAIN GATE SOURCE BULK (84 45 86 47)
M39 Vss 18 34 999 NMOS L=5u W=65u
* M39 DRAIN GATE SOURCE BULK (91 69 101 81)
M40 34 Vdd Vdd 999 NMOS L=5u W=5u
* M40 DRAIN GATE SOURCE BULK (84 75 86 77)
M41 17 U10/Vp2 34 999 NMOS L=5u W=15u
* M41 DRAIN GATE SOURCE BULK (92 63 98 65)
M42 21 U10/Vp2 33 999 NMOS L=5u W=15u
* M42 DRAIN GATE SOURCE BULK (52 69 58 71)
M43 Vss 19 37 999 NMOS L=5u W=65u
* M43 DRAIN GATE SOURCE BULK (91 99 101 111)
M44 37 Vdd Vdd 999 NMOS L=5u W=5u
* M44 DRAIN GATE SOURCE BULK (84 105 86 107)
M45 Vss 20 36 999 NMOS L=5u W=65u
* M45 DRAIN GATE SOURCE BULK (91 129 101 141)
M46 36 Vdd Vdd 999 NMOS L=5u W=5u
* M46 DRAIN GATE SOURCE BULK (84 135 86 137)
M47 20 U10/Vp1 U7/Vb 999 NMOS L=5u W=15u
* M47 DRAIN GATE SOURCE BULK (92 153 98 155)
M48 Vss 21 32 999 NMOS L=5u W=65u
* M48 DRAIN GATE SOURCE BULK (49 83 59 95)
M49 Vdd Vdd 32 999 NMOS L=5u W=5u
* M49 DRAIN GATE SOURCE BULK (64 87 66 89)
M50 Vss 22 33 999 NMOS L=5u W=65u
* M50 DRAIN GATE SOURCE BULK (49 53 59 65)
M51 Vdd Vdd 33 999 NMOS L=5u W=5u
* M51 DRAIN GATE SOURCE BULK (64 57 66 59)
M52 U7/Vout U10/Vp1 22 999 NMOS L=5u W=15u
* M52 DRAIN GATE SOURCE BULK (52 39 58 41)
M53 Vss 23 U7/Vb 999 NMOS L=5u W=65u
* M53 DRAIN GATE SOURCE BULK (49 143 59 155)
M54 Vdd Vdd U7/Vb 999 NMOS L=5u W=5u
* M54 DRAIN GATE SOURCE BULK (64 147 66 149)
M55 Vss 24 35 999 NMOS L=5u W=65u
* M55 DRAIN GATE SOURCE BULK (49 113 59 125)
M56 Vdd Vdd 35 999 NMOS L=5u W=5u
* M56 DRAIN GATE SOURCE BULK (64 117 66 119)
M57 24 U10/Vp1 32 999 NMOS L=5u W=15u
* M57 DRAIN GATE SOURCE BULK (52 99 58 101)
M58 U7/U3/drain U7/Vb Vss 999 NMOS L=5u W=135u
* M58 DRAIN GATE SOURCE BULK (76 187 90 205)

M59 Vss U7/Va U7/U3/drain 999 NMOS L=5u W=140u
* M59 DRAIN GATE SOURCE BULK (92 189 112 203)
M60 U7/U0/drain U7/Vb Vss 999 NMOS L=5u W=135u
* M60 DRAIN GATE SOURCE BULK (90 165 110 181)
M61 U7/Vout 28 U7/U3/drain 999 NMOS L=5u W=135u
* M61 DRAIN GATE SOURCE BULK (118 191 138 207)
M62 Vdd Vdd U7/Vout 999 NMOS L=5u W=5u
* M62 DRAIN GATE SOURCE BULK (141 197 143 199)
M63 Vdd Vdd 28 999 NMOS L=5u W=5u
* M63 DRAIN GATE SOURCE BULK (141 174 143 176)
M64 Vss Vss Vrst 999 NMOS L=5u W=505u
* M64 DRAIN GATE SOURCE BULK (2 2 78 17)
M65 Vss Vrst U7/Vout 999 NMOS L=5u W=15u
* M65 DRAIN GATE SOURCE BULK (52 29 58 31)

* Total Nodes: 38
* Total Elements: 65
* Extract Elapsed Time: 2 seconds
.END

APPENDIX C – LAYOUT VS. SCHEMATIC OUTPUT

File written by LVS 3.13/Win32 as a result of: "W:\Project\LVS\Project.vdb" on Sat Dec 18 18:26:07 2004

Command line:

```
lvs W:\Project\SPICE\JW_PS.cir W:\Project\LVS\Project.net -o W:\Project\LVS\LVS.out  
-pspice -nrcl -c2 -dg15.000 -vfa
```

Engine configuration report:

```
Consider Bulk nodes.....ON  
Consider Resistors as polarized elements.....OFF  
Consider Capacitors as polarized elements.....OFF  
Consider Inductors as polarized elements.....OFF  
Optimize shorted & parallel R, C, MOSFETs; series R and C.....OFF  
Replace series MOSFETs.....OFF  
Fast Iteration.....OFF
```

Parsing file W:\Project\SPICE\JW_PS.cir...

Flattening network...

Parsing file W:\Project\LVS\Project.net...

Flattening network...

Device	JW_PS.cir	Project.net
M_NMOS	65	65
Total elements	65	65
Total nodes	39	39

Iterating...

5% done

10% done

Warning: Parametric mismatch between elements JW_PS.cir: M2:L=5e-006 W=5.5e-005 (Not all decimals shown) and Project.net: M_OutputBuffer_M4:L=5e-006 W=4.5e-005 (Not all decimals shown)

Warning: Parametric mismatch between elements JW_PS.cir: M4:L=5e-006 W=7.25e-005 (Not all decimals shown) and Project.net: M_OutputBuffer_M2:L=5e-006 W=6e-005 (Not all decimals shown)

15% done
20% done
25% done
30% done
35% done
40% done
45% done
50% done
55% done
60% done
65% done
70% done
75% done
80% done
85% done
90% done
95% done

***** REPORTING AUTOMORPHISM *****

Report of elements:

Automorph class of elements

JW_PS.cir	M8	fanout: BULK = 64	D/S (4, 31)	G = 3
JW_PS.cir	M7	fanout: BULK = 64	D/S (4, 31)	G = 3
Project.net	M_OutputBuffer_M8	fanout: BULK = 64	D/S (4, 31)	G = 3
Project.net	M_OutputBuffer_M3	fanout: BULK = 64	D/S (4, 31)	G = 3

63 perfectly matched element class(es)
1 automorphed element class(es)
39 perfectly matched node class(es)

Doing detailed trial matching...
100% done

Circuits are only topologically equal.
Run time: 0:02 (min:sec)

0 error(s), 2 warning(s)