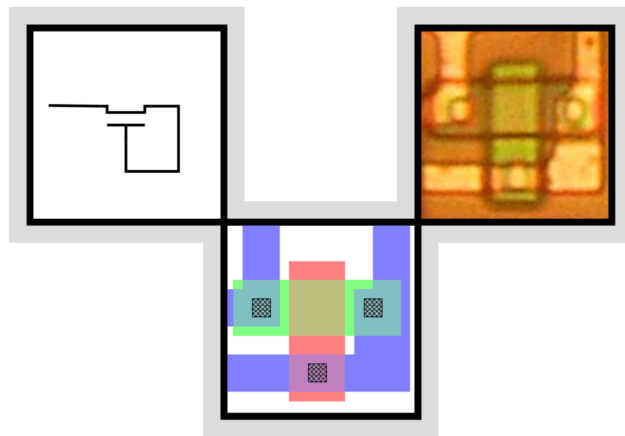
Carleton
UNIVERSITY

ELEC 4609 Notes



Professor N. G. Tarr

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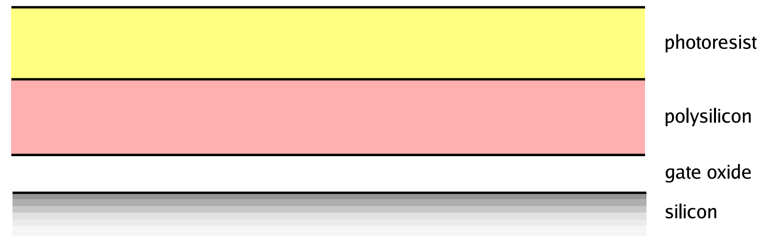
1 Introduction to MOS Technology

1.1 Basic MOS Process Flow

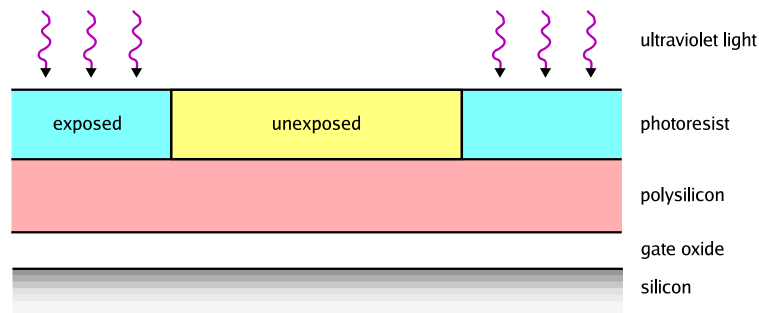
- thick field oxide provides isolation between transistors by blocking phosphorus diffusion into silicon
- layers of materials are patterned using a technique called *photolithography*

  Example of photolithography: patterning of polysilicon gate (step [e] in following section).

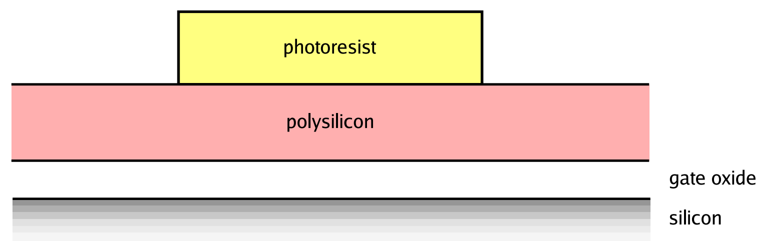
1. Apply organic photosensitive material called *photoresist* uniformly over wafer surface.



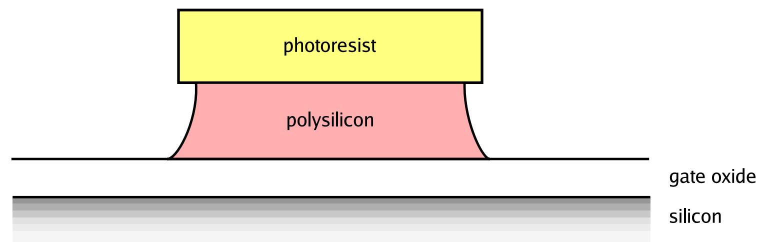
2. Press photoresist-coated wafer into contact with a glass plate having opaque and transparent regions (called a *photomask*). Expose photomask and wafer to a bright ultraviolet light source (effectively a contact printing process). Where photoresist is exposed to light, it changes chemically and becomes soluble in a dilute alkaline solution. Unexposed photoresist remains insoluble.



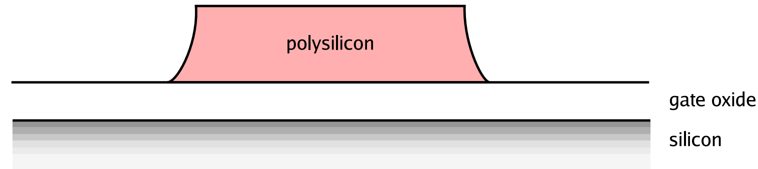
3. Develop photoresist by immersing wafer in alkaline solution.



4. Etch polysilicon (for example, immerse wafer in hydrofluoric acid/nitric acid solution; many other techniques are available).



5. Remove photoresist (e.g. immerse wafer in acetone).



Photolithography is repeated four times in the basic ELEC 4609 process. In modern CMOS technology, 20 or more lithography steps might be required.

1.2 Carleton's $5\mu m$ Poly Gate, LOCOS-isolated nMOS Process

The starting material is: p-type, (100) orientation, $2\Omega cm$ resistivity.

Device isolation

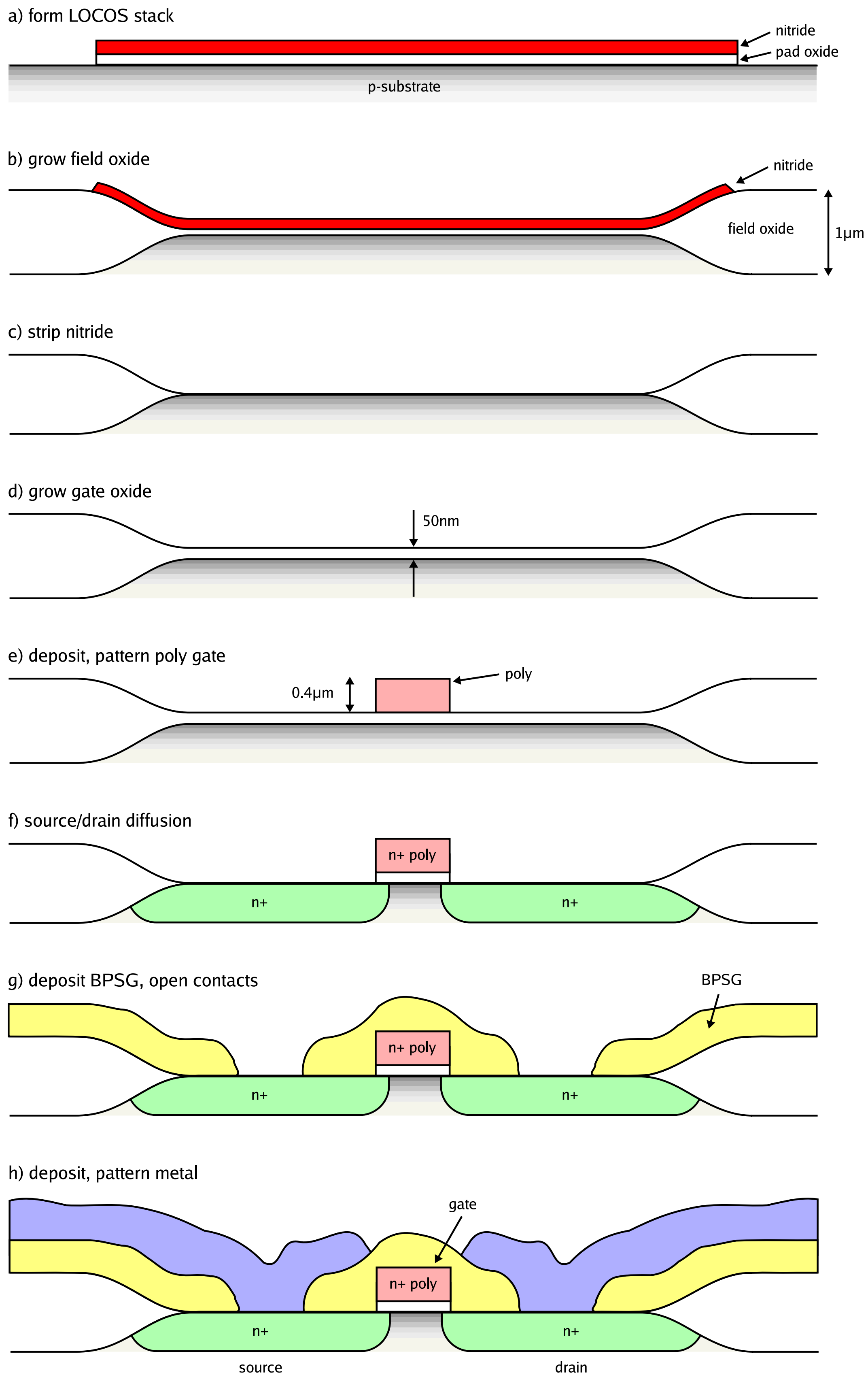
- Grow pad oxide ($80nm$): $1100°C$ dry O_2
- Deposit silicon nitride
- Pattern nitride and pad oxide (PE#1: device well) [a]
- Grow field oxide ($1\mu m$): $1100°C$ wet O_2 [b]
- Strip nitride and pad oxide [c]

Active Device Formation

- Grow gate oxide ($50nm$): $1100°C$ dry O_2 [d]
- Deposit gate polysilicon ($0.4\mu m$) by LPCVD
- Pattern polysilicon gates and interconnects (PE#2: poly) [e]
- Diffuse source and drain regions: $1000°C$ $POCl_3$ [f]

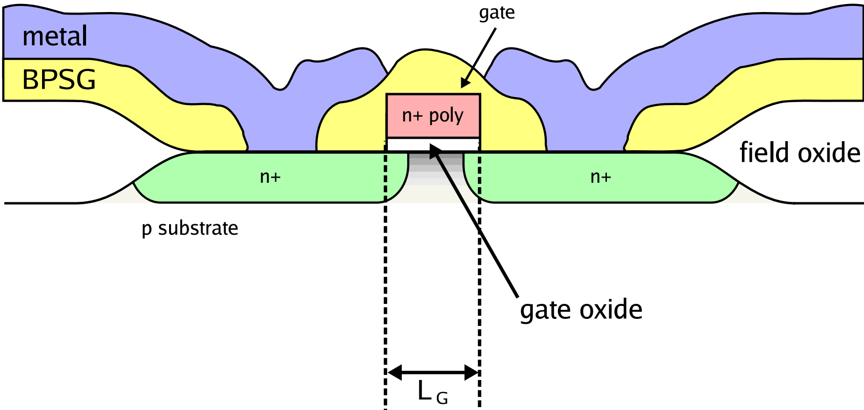
Device Interconection

- Deposit intermediate dielectric ($0.5\mu m$ BPSG)
- Flow dielectric to smooth topography ($900°C$, 30 minutes)
- Open contact windows (PE#3: contacts) [g]
- Deposit front contact metal ($1\mu m$ Al by e-beam)
- Pattern front metal (PE#4: metal) [h]
- Sinter metal contacts: $450°C$ H_2
- Strip oxide from wafer backs
- Deposit $1\mu m$ Al on wafer backs

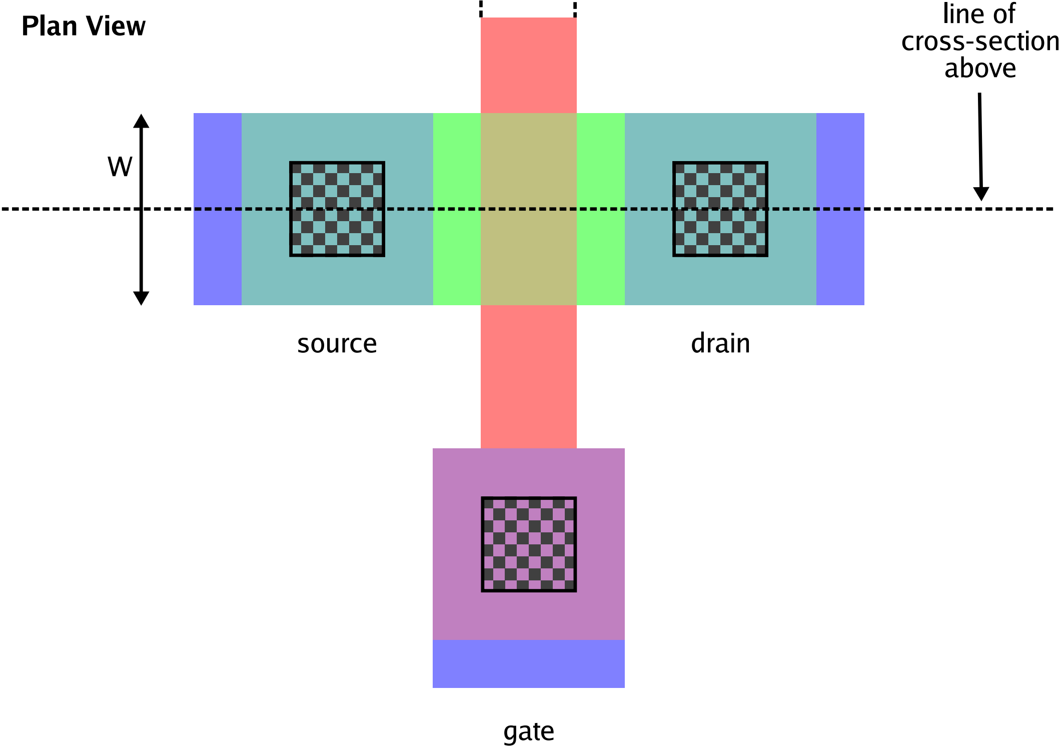


a) form LOCOS stack
nitride
pad oxide
p-substrate
b) grow field oxide
nitride
field oxide
1μm
c) strip nitride
d) grow gate oxide
50nm
e) deposit, pattern poly gate
0.4μm
poly
f) source/drain diffusion
n+ poly
n+
n+
g) deposit BPSG, open contacts
BPSG
n+ poly
n+
n+
h) deposit, pattern metal
gate
n+ poly
n+
n+
source
drain

Cross Section



Plan View



1.3 MOSFET Layout

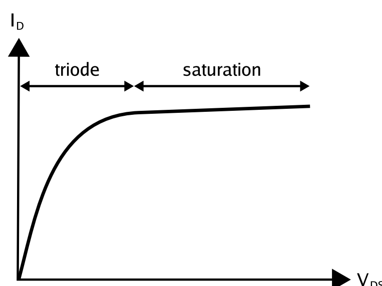
To build a MOSFET in the basic ELEC 4609 nMOS process, the IC designer must specify the size, shape, and relative alignment of the following four layers to obtain the correct device electrical characteristics:

- device well
- polysilicon
- contact
- metal

These are the layers patterned in the four photolithography steps.

The size and shape of the device well and polysilicon determine the length L and width W of MOSFETs.

Simple SPICE level 1 for MOSFET:



Saturation:

$$I_D = \frac{W}{L}\mu_n C_{ox}\frac{(V_{GS}-V_T)^2}{2}$$

Triode:

$$I_D = \frac{W}{L}\mu_n\left(C_{ox}V_{GS}-V_T-\frac{V_{DS}}{2}\right)$$

where $C_{ox}=\frac{t_o}{t_{ox}}$, t_{ox} = gate oxide thickness, and $\mu_n \cong 600cm^2V^{-1}s^{-1}$.

$$V_T = V_{FB} + 2\phi_B + \frac{\sqrt{2\epsilon_S q N_A(2\phi_B)}}{C_{ox}}$$

where $\phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$.

Typically V_T varies between 0.5 and 0.7V. $\phi_B \cong 0.3$ to 0.4V. V_{FB}, N_A, and t_{ox} are fixed for a given process technology.

Therefore, once a technology is chosen, the only way an IC designer can control the electrical characteristics of a MOSFET is through the $\frac{W}{L}$ ratio.

1.4 Design Rules

1.4.1 Mead-Conway

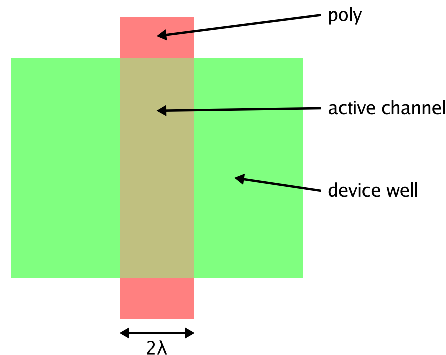
Size and spacing of the layers making up an IC cannot be chosen arbitrarily; they must satisfy certain design rules. Design rules are generally process dependent. Each new technology has a new set of design rules to learn. Commercial design rules are often very complex, with dozens of pages of documentation.

In the late 1970's, when classes at CalTech first started to design integrated circuits, Carver Mead and Lynn Conway introduced the concept of simplified design rules, in which all rules are expressed in terms of integer multiples of a basic length λ.

Mead-Conway rules have the advantage that it is usually possible to scale designs from one technology generation to the next, simply by reducing λ. For ELEC 4609 nMOS, $\lambda = 2.5\mu m$.

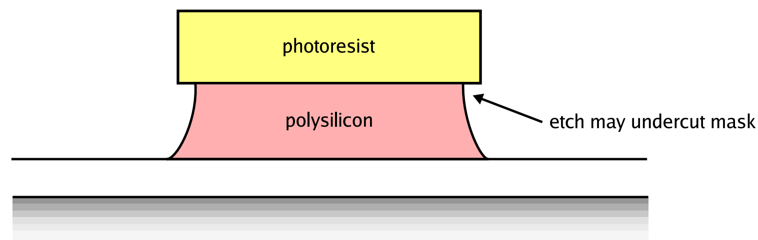
1.4.2 Examples of Design Rules

1. Minimum poly length $= 2\lambda = 5\mu m$ (rule 1b). This determines the minimum MOSFET length.

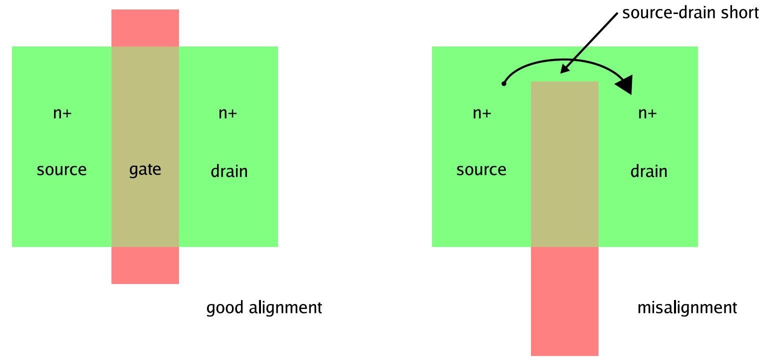


   Reasons for rule:

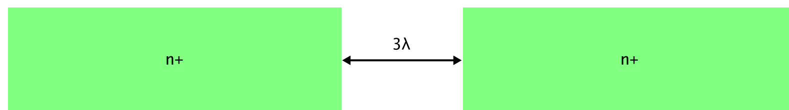
   - limited resolution of photolithographic printing process (depends on wavelength of ultraviolet light, quality of optics, etcetera).
   - loss of feature domensions during etching due to undercut (depends on etching technique).

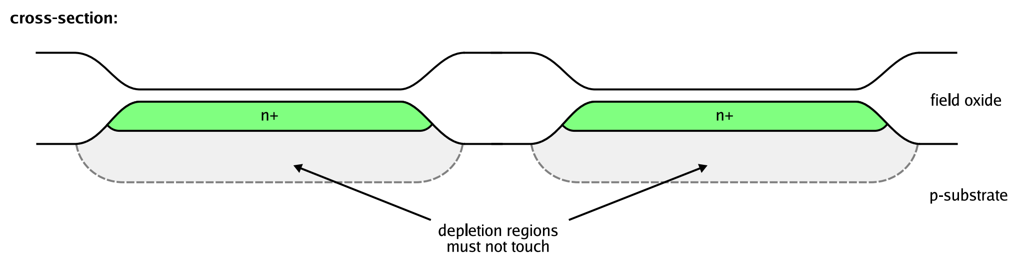


2. Poly must overlap device well by at least 2λ (rule 4a). This is determined primarily by accuracy of level-to-level registration. For example, in Carleton nMOS, a human aligns the poly mask to the device well manually using a microscope.



3. Minimum device well - device well spacing = 3λ

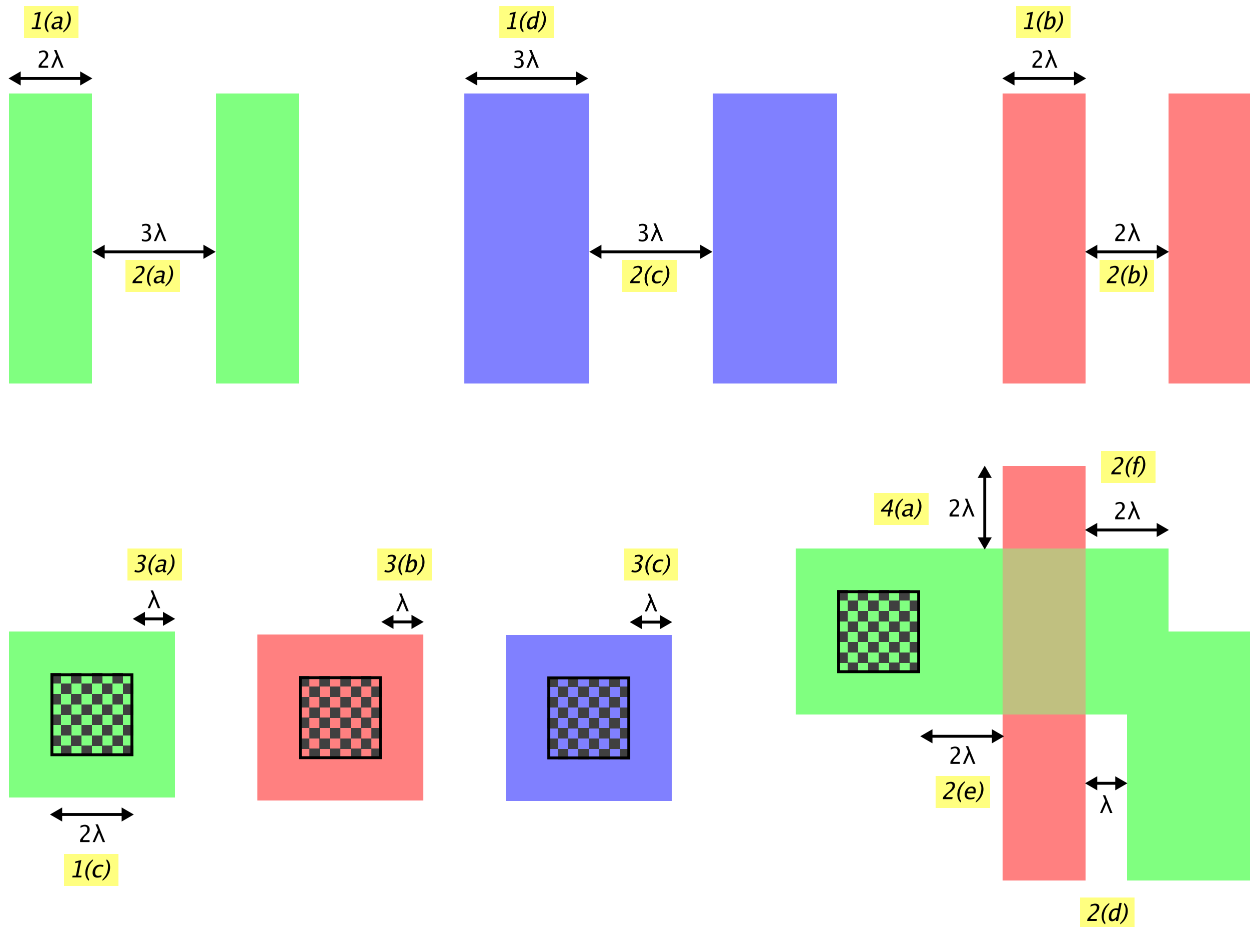




The depletion width is described as:

$$W = \sqrt{\frac{2\epsilon(2\phi_B + V)}{qN_A}}$$

For ELEC 4609 nMOS, with $V = 5V$, W may approach $1\mu m$, meaning that extra spacing must be allowed to provide room for depletion region.



Mead-Conway Design Rules

1. Minimum widths:
   (a) device well: 2λ
   (b) poly: 2λ
   (c) contact: 2λ
   (d) metal: 3λ (4λ recommended)

2. Minimum spacings:
   (a) device well - device well: 3λ
   (b) poly - poly: 2λ
   (c) metal - metal: 3λ (4λ recommended)
   (d) poly - device well: 1λ
   (e) contact - active channel: 2λ
   (f) poly - device well: 2λ (poly inside device well)

3. Minimum enclosures:
   (a) device well surrounding contact: 1λ
   (b) poly surrounding contact: 1λ
   (c) metal surrounding contact: 1λ

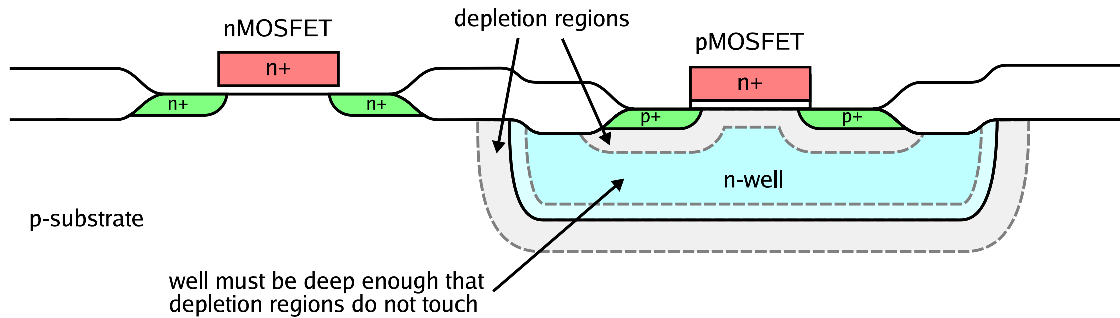
4. Minimum overlap:
   (a) poly overlapping device well: 2λ

1.5 Basic CMOS Technology

The simplest possible MOS process needs only 4 photolithography steps, but produces only n-channel MOSFETS. There are major advantages to having both n- and p-channel transistors available for both digital and analog circuit designs. This is why CMOS technology is needed.

Simple approach to CMOS:

- Use basic ELEC 4609 nMOS technology.
- Early in the process flow add a phosphorus implant followed by a long phosphorus diffusion to form an n-well.
- Build p-channel transistors in the n-wells.



Some points to note:

- In older CMOS technologies, the p-channel MOSFETs have n^+ gates. This is possible because the gate polysilicon is saturated with phosphorus before it is patterned, and the solid solid solubility of phosphorus in silicon is greater than that of boron.
- The simplest CMOS technology needs 7 masks, compared to 4 for the simplest nMOS technology. A mask is needed to form the n-well, and the source-drain doping of the n- and p-channel transistors must be done separately, requiring two more masks.

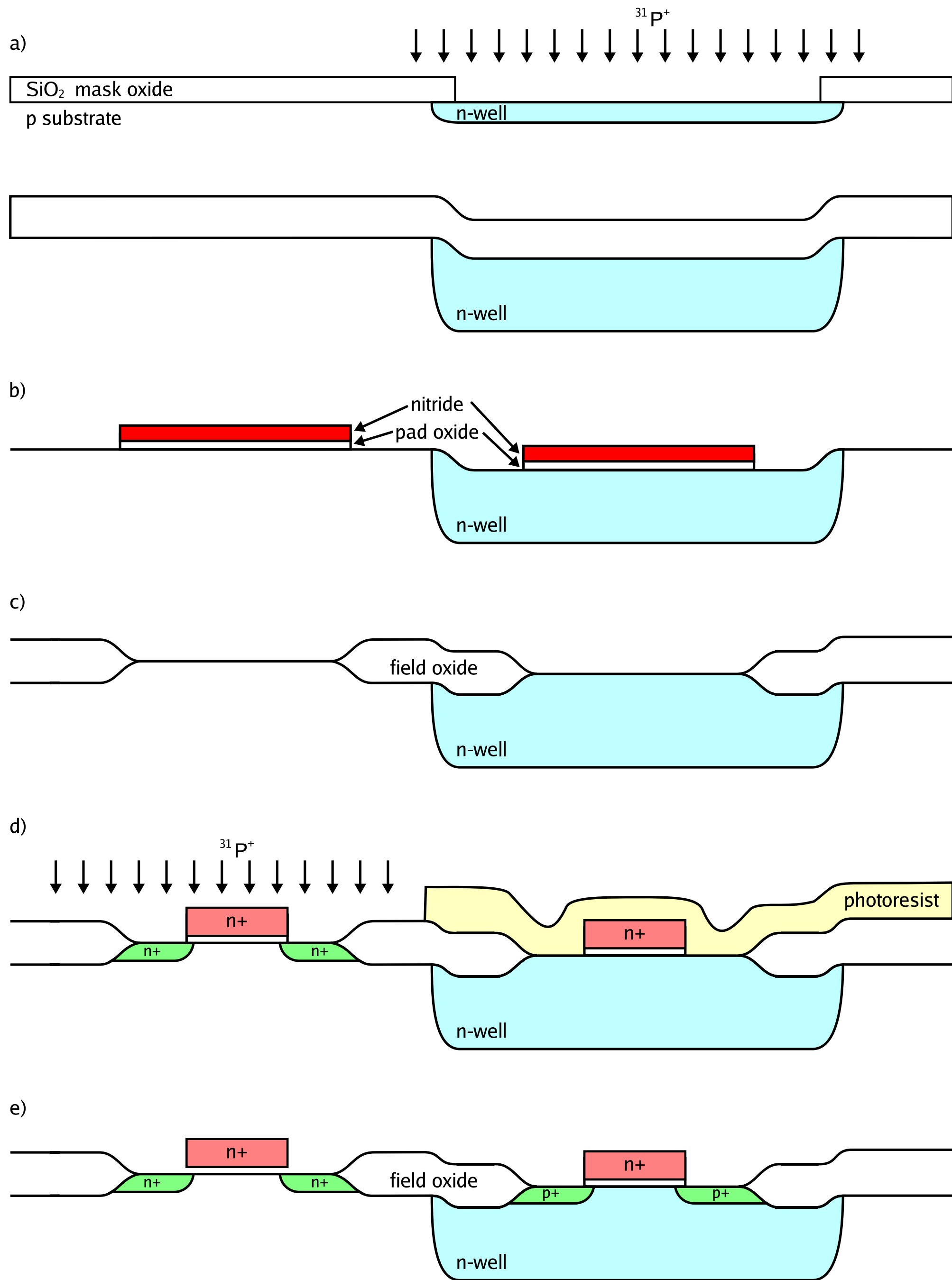
1.6 Basic N-Well CMOS Technology

Simplified process flow

Starting material: lightly-doped p-type silicon wafer

1. N-Well Formation
   (a) Mask oxidation
   (b) N-well PE and oxide etch [PE 1]
   (c) N-well phosphorus implant (Figure a)
   (d) N-well oxidation and drive-in
2. Device Isolation
   (a) Blanket oxide etchback
   (b) Pad oxidation
   (c) Nitride deposition
   (d) Device well PE and etch (Figure b) [PE 2]
   (e) Field exidation
3. Active Device Formation
   (a) Blanket nitride and pad oxide etchback (Figure c)
   (b) Gate oxidation
   (c) Gate polysilicon deposition
   (d) Blanket N+ phosphorus diffusion to dope gate
   (e) Gate PE and etch [PE 3]
   (f) N+ PE [PE 4]
   (g) N+ phosphorus implant (Figure d)
   (h) P+ PE [PE 5]
   (i) P+ boron implant
   (j) Source/drain implant anneal (Figure e)
4. Contact and Interconnect Formation
   (a) BPSG deposition
   (b) Contact PE and etch [PE 6]
   (c) Metal deposition
   (d) Metal PE and etch [PE 7]
   (e) Passivation oxide deposition
   (f) Bond pad PE and etch [PE 8]

At least one extra PE (photoetch) and implant is often required to adjust the threshold of the parasitic field transistors to ensure they never turn on. Modern processes use several levels of metal, separated by layers of deposited oxide.


a)
$^{31}P^+$
SiO_2 mask oxide
p substrate
n-well
n-well
b)
nitride
pad oxide
n-well
c)
field oxide
n-well
d)
$^{31}P^+$
n+
n+
n+
photoresist
n+
n-well
e)
n+
n+
n+
field oxide
p+
n+
p+
n-well